

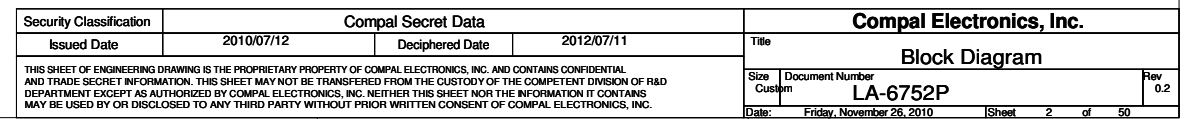
Compal Confidential

G470/G570 UMA M/B Schematics Document

Intel Sandy Bridge Processor with DDRIII + Cougar Point PCH

2010-10-22
LA-6752P / LA-6754P
REV: 0.2

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Voltage Rails

power plane	State	+B	+5VALW +3VALW	+1.5V	+5VS +3VS +1.5VS +VCCP +CPU_CORE +VGA_CORE +GFX_CORE +1.8VS +0.75VS +1.05VS
S0		○	○	○	○
S3		○	○	○	✗
S5 S4/AC		○	○	✗	✗
S5 S4/ Battery only		○	✗	✗	✗
S5 S4/AC & Battery don't exist		✗	✗	✗	✗

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	Thermal Sensor EMC1403-2	1001_101xb

PCH SM Bus address

Device	Address
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

SMBUS Control Table

	SOURCE	VGA	BATT	KE930	SODIMM	WLAN WWAN	Thermal Sensor	PCH
SMB_EC_CK1	KB930	✗	✓	✗	✗	✗	✗	✗
SMB_EC_DA1	+3VALW		+3VALW					
SMB_EC_CK2	KB930	✗	✗	✗	✗	✗	✗	✓
SMB_EC_DA2	+3VALW							+3VS
SMBCLK	PCH	✗	✗	✗	✓	✓	✗	✗
SMBDATA	+3VALW				+3VS	+3VS		
SML0CLK	PCH	✗	✗	✗	✗	✗	✗	✗
SML0DATA	+3VALW							
SML1CLK	PCH	✓	✗	✓	✗	✗	✓	✗
SML1DATA	+3VALW	+3VS		+3VS			+3VS	

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	
2	
3	
4	
5	
6	
7	

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%				
Ra/Rc/Re	100K +/- 5%				
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max	
0	0	0 V	0 V	0 V	EVT
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V	DVT
2	18K +/- 5%	0.436 V	0.503 V	0.538 V	PVT
3	33K +/- 5%	0.712 V	0.819 V	0.875 V	MP
4	56K +/- 5%	1.036 V	1.185 V	1.264 V	
5	100K +/- 5%	1.453 V	1.650 V	1.759 V	
6	200K +/- 5%	1.935 V	2.200 V	2.341 V	
7	NC	2.500 V	3.300 V	3.300 V	

USB Port Table

USB 2.0	USB 1.1	Port	3 External USB Port
EHCI1	UHCI0	0	USB/B (Right Side)
		1	USB Port (Left Side)
	UHCI1	2	USB Port (Left Side)
		3	USB Port (Left Side)
	UHCI2	4	
		5	Camera
	UHCI3	6	
EHCI2		7	
	UHCI4	8	Mini Card(WLAN)
		9	
	UHCI5	10	
		11	Card Reader
	UHCI6	12	
		13	Blue Tooth

BOM Structure Table

BTO Item	BOM Structure
CAMERA DEVICE	CMOS@
Blue Tooth	BT@
eSATA	ESATA@
COMMON HDMI	HDMI@
Connector	ME@
45 LEVEL	45@
10/100 LAN	8152@
GIGA LAN	GIGA@
Unpop	@

Power-Up/Down Sequence

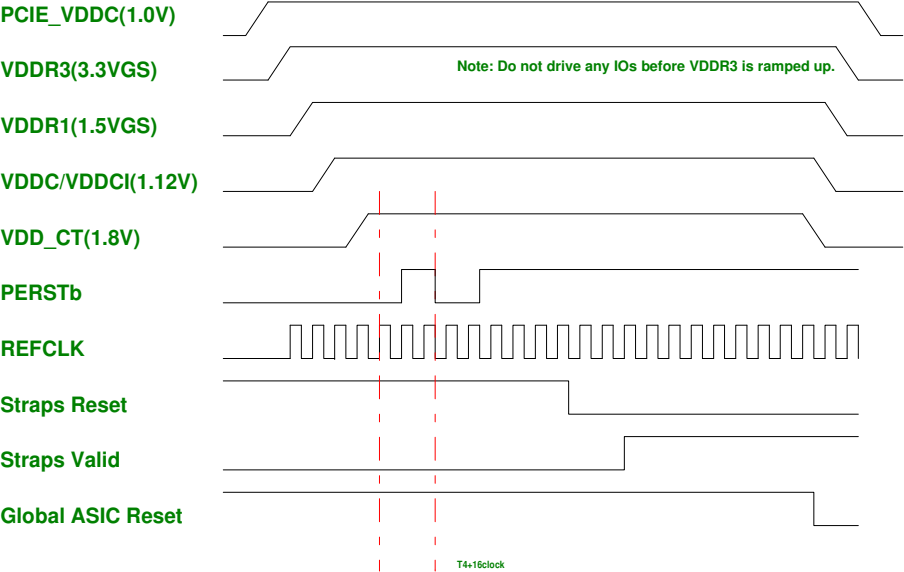
All the ASIC supplies must fully reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred.

VDDR3 should ramp-up before or simultaneously with VDDC.

For LVDS, DPx_VDD10 should ramp-up before DPx_VDD18 and the PCIe Reference clock should begin before DPx_VDD18. For power-down, DPx_VDD18 should ramp-down before DPx_VDD10.

The external pull-ups on the DDC/AUX signals (if applicable) should ramp-up before or after both VDDC and VDD_CT have ramped up.

VDDC and VDD_CT should not ramp-up simultaneously. (e.g., VDDC should reach 90% before VDD_CT starts to ramp-up (or vice versa).)



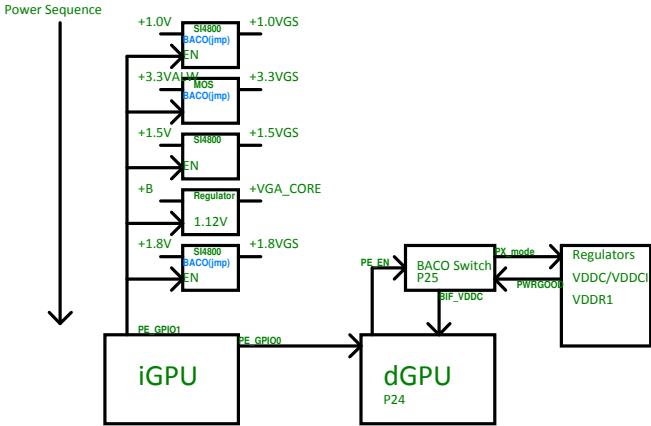
Without BACO option :

- PE_GPIO0 : Low -> Reset dGPU ; High ->Normal operation
- PE_GPIO1 : Low -> dGPU Power OFF ; High -> dGPU Power ON

BACO option :

- PE_GPIO0 : High ->Normal operation (dGPU is not reseton BACO mode)
- PE_GPIO1 : Low -> dGPU Power OFF ; High -> dGPU Power ON (always High)

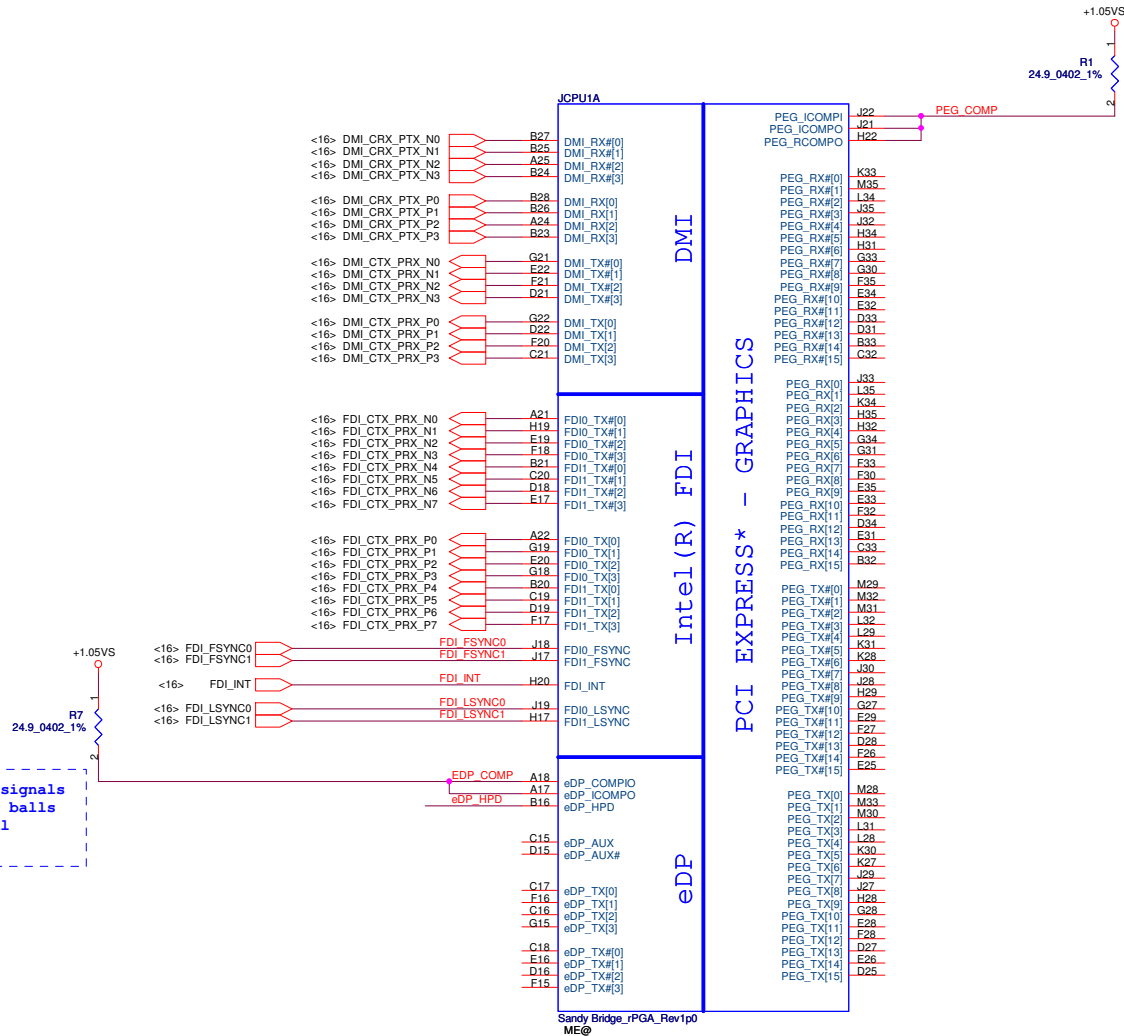
dGPU Power Pins	Voltage	PX 3.0	BACO Mode	Max current
PCIe_PVDD, PCIe_VDDR, TSVDD, VDDR4, VDD_CT, DPE_PVDD, DP[F:E]_VDD18, DP[D:A]_PVDD, DP[D:A]_VDD18, AVDD, VDD1DI, A2VDDQ, VDD2DI, DPLL_PVDD, MPV18, and SPV18	1.8V	OFF	ON	1679mA
DP[F:E]_VDD10, DP[D:A]_VDD10, DPLL_VDDC, and SPV10	1.0V	OFF	ON	575mA
PCIe_VDDC	1.0V	OFF	ON	2A
VDDR3 , and A2VDD	3.3V	OFF	ON	190mA
BIF_VDDC (current consumption = 55mA@1.0V, in BACO mode)	Same as VDDC	OFF	ON Same as PCIe_VDDC	70mA
VDDR1	1.5V	OFF	OFF	2.8A
VDDC/VDDCI	1.12V	OFF	OFF	12.9A



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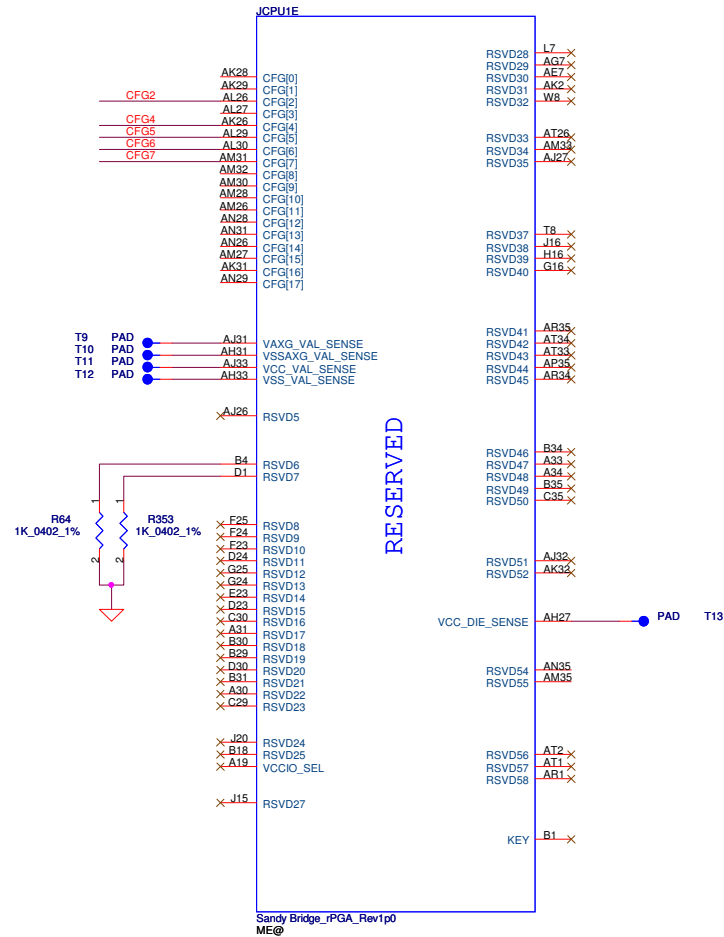
eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

PEG_ICOMPI and RCOMPO signals should be shorted and routed with - max length = 500 mils - typical impedance = 43 mohms
PEG_ICOMPO signals should be routed with - max length = 500 mils - typical impedance = 14.5 mohms

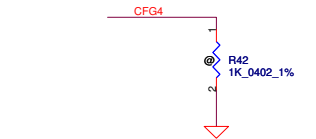


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				PROCESSOR(1/7) DMI,FDI,PEG					
				Size		Document Number	Rev		
				Custom		LA-6752P	0.2		
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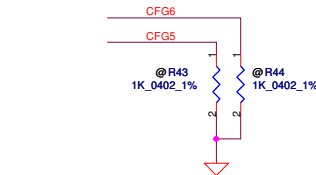
CFG Straps for Processor



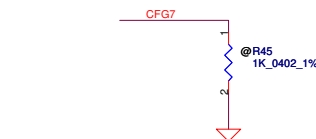
PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition * 0: Lane Reversed



Display Port Presence Strap	
CFG4	* 1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

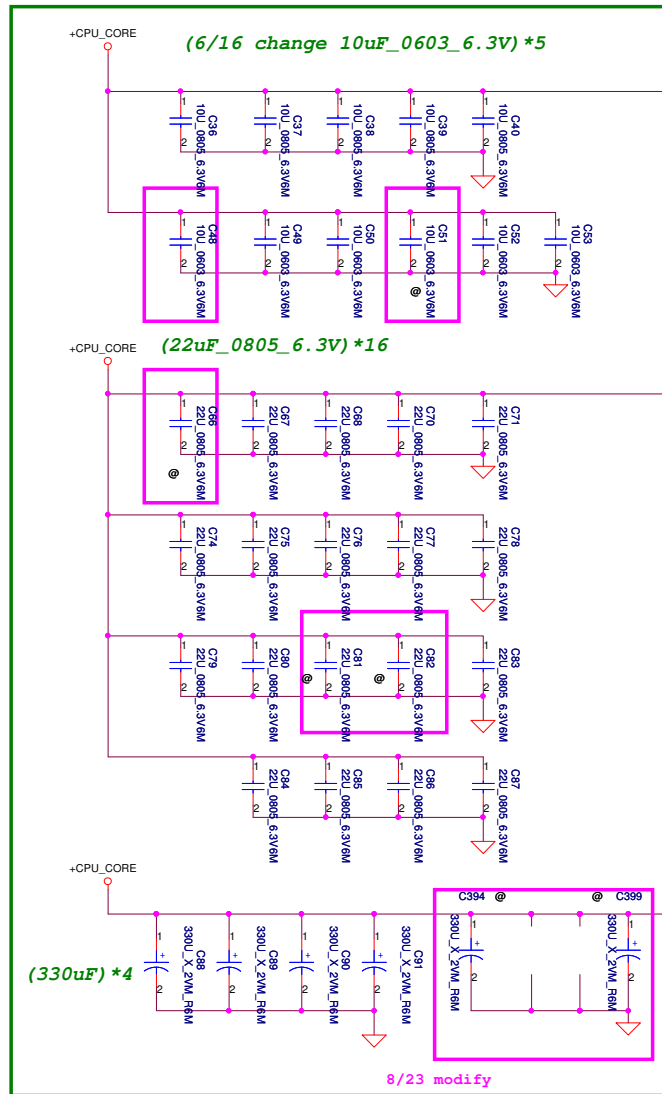


PCIe Port Bifurcation Straps	
CFG[6:5]	* 11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

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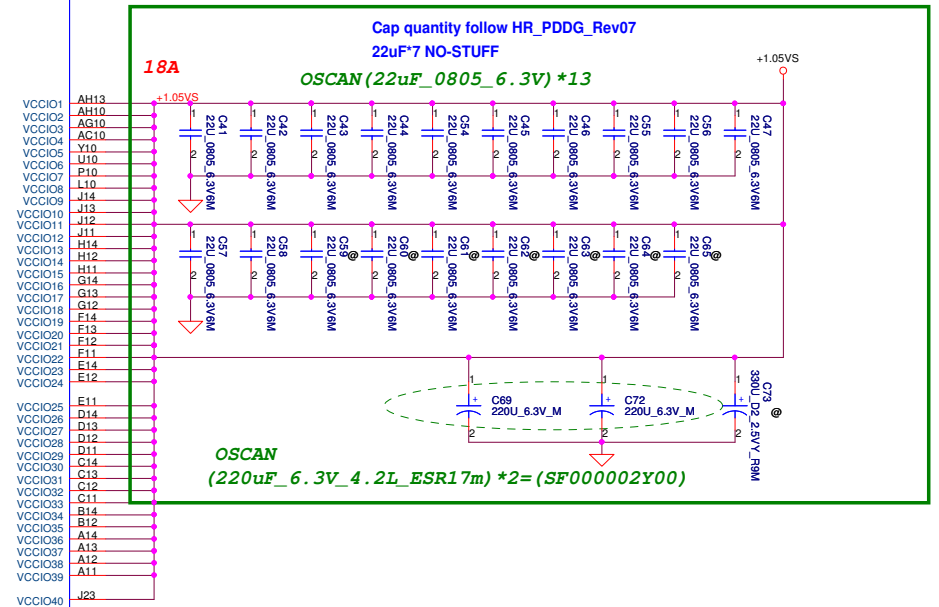


QC=94A
DC=53A

AG35	VCC1
AG34	VCC2
AG33	VCC3
AG32	VCC4
AG31	VCC5
AG30	VCC6
AG29	VCC7
AG28	VCC8
AG27	VCC9
AG26	VCC10
AF35	VCC11
AF34	VCC12
AF33	VCC13
AF32	VCC14
AF31	VCC15
AF30	VCC16
AF29	VCC17
AF28	VCC18
AF27	VCC19
AF26	VCC20
AD35	VCC21
AD34	VCC22
AD33	VCC23
AD32	VCC24
AD31	VCC25
AD30	VCC26
AD29	VCC27
AD28	VCC28
AD27	VCC29
AD26	VCC30
AC35	VCC31
AC34	VCC32
AC33	VCC33
AC32	VCC34
AC31	VCC35
AC30	VCC36
AC29	VCC37
AC28	VCC38
AC27	VCC39
AC26	VCC40
AA35	VCC41
AA34	VCC42
AA33	VCC43
AA32	VCC44
AA31	VCC45
AA30	VCC46
AA29	VCC47
AA28	VCC48
AA27	VCC49
Y35	VCC50
Y34	VCC51
Y33	VCC52
Y32	VCC53
Y31	VCC54
Y30	VCC55
Y29	VCC56
Y28	VCC57
Y27	VCC58
Y26	VCC59
Y25	VCC60
Y24	VCC61
Y23	VCC62
Y22	VCC63
Y21	VCC64
Y20	VCC65
Y19	VCC66
Y18	VCC67
Y17	VCC68
Y16	VCC69
Y15	VCC70
Y14	VCC71
Y13	VCC72
Y12	VCC73
Y11	VCC74
Y10	VCC75
Y09	VCC76
Y08	VCC77
Y07	VCC78
Y06	VCC79
Y05	VCC80
Y04	VCC81
Y03	VCC82
Y02	VCC83
Y01	VCC84
Y00	VCC85
Y00	VCC86
Y00	VCC87
Y00	VCC88
Y00	VCC89
Y00	VCC90
Y00	VCC91
Y00	VCC92
Y00	VCC93
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Y00	VCC95
Y00	VCC96
Y00	VCC97
Y00	VCC98
Y00	VCC99
Y00	VCC100

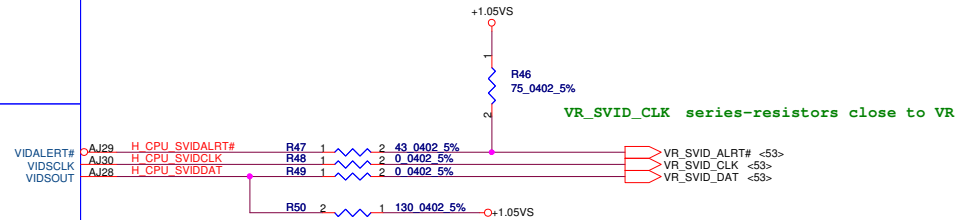
POWER

PEG AND DDR

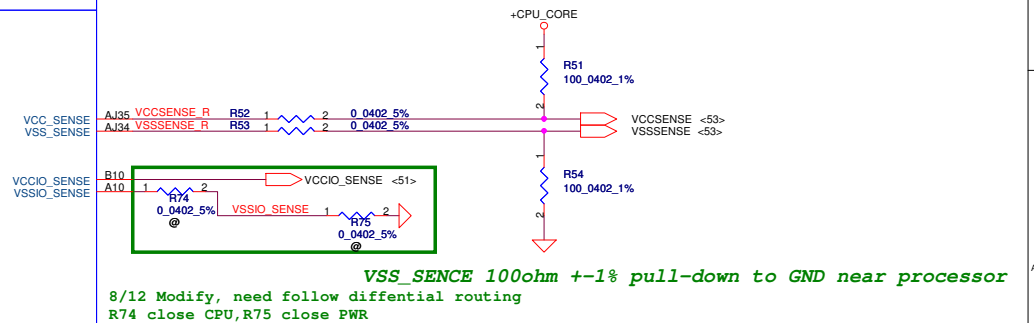


CORE SUPPLY

SVID



SENSE LINES

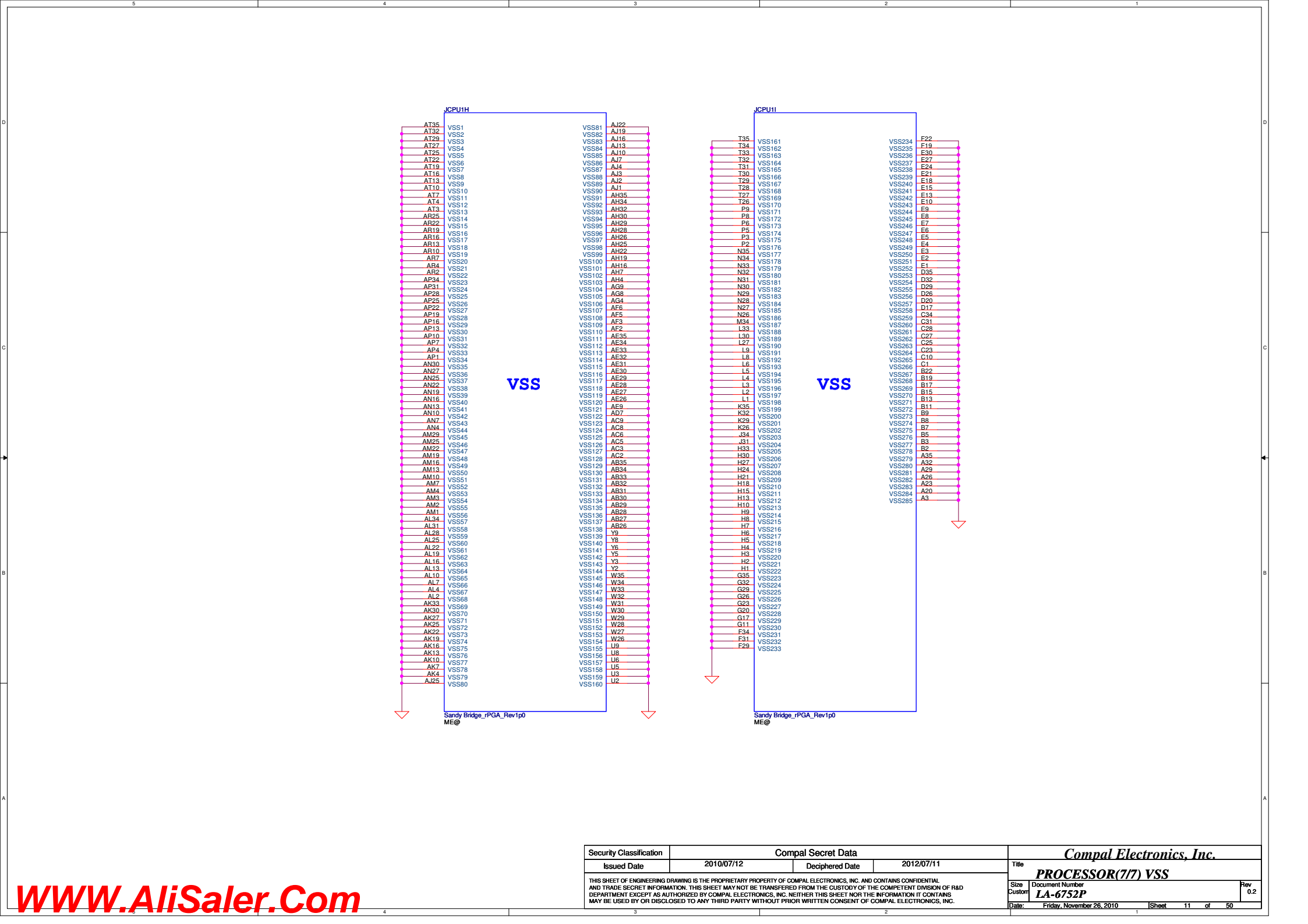


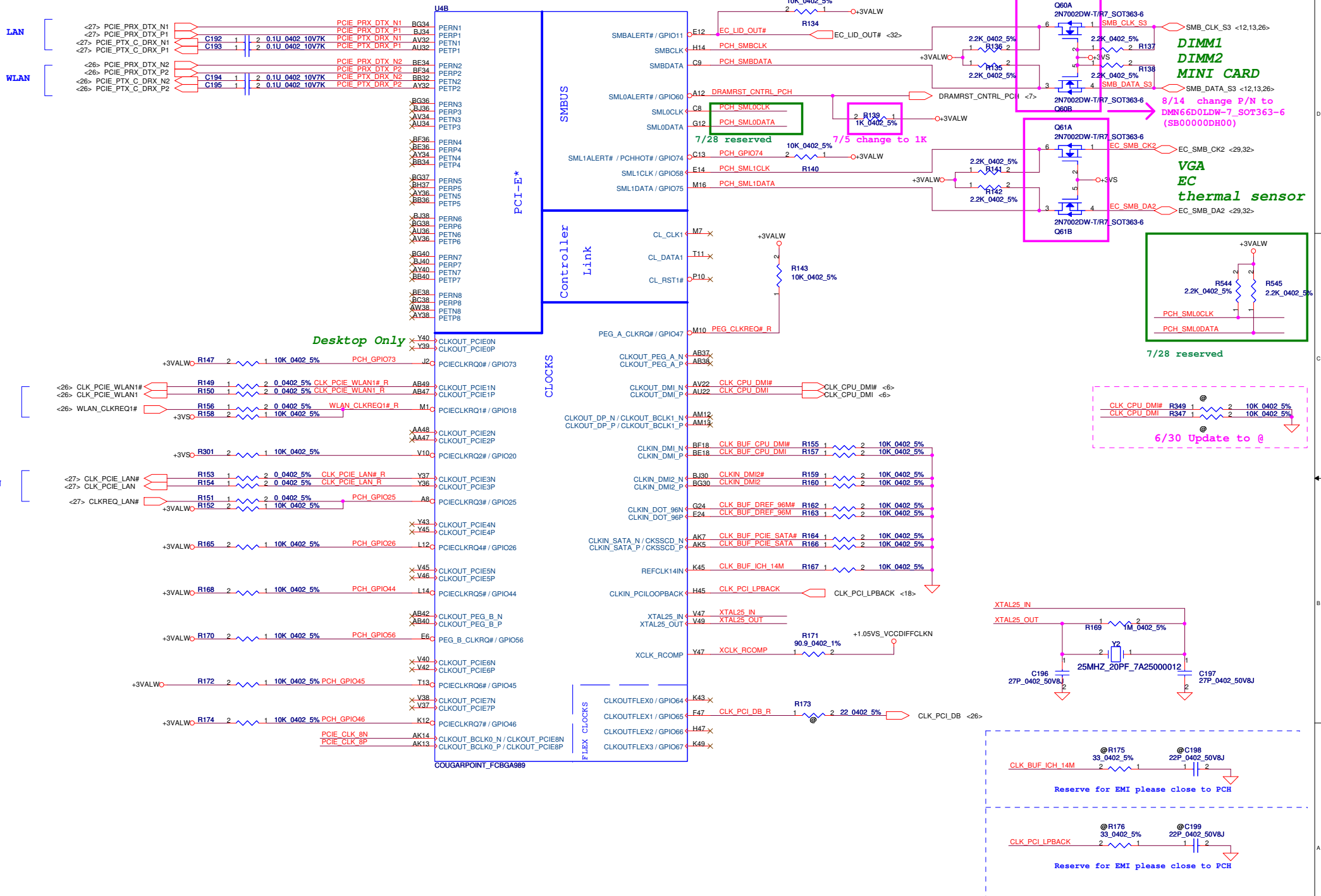
Sandy Bridge_rPGA Rev10A
ME@

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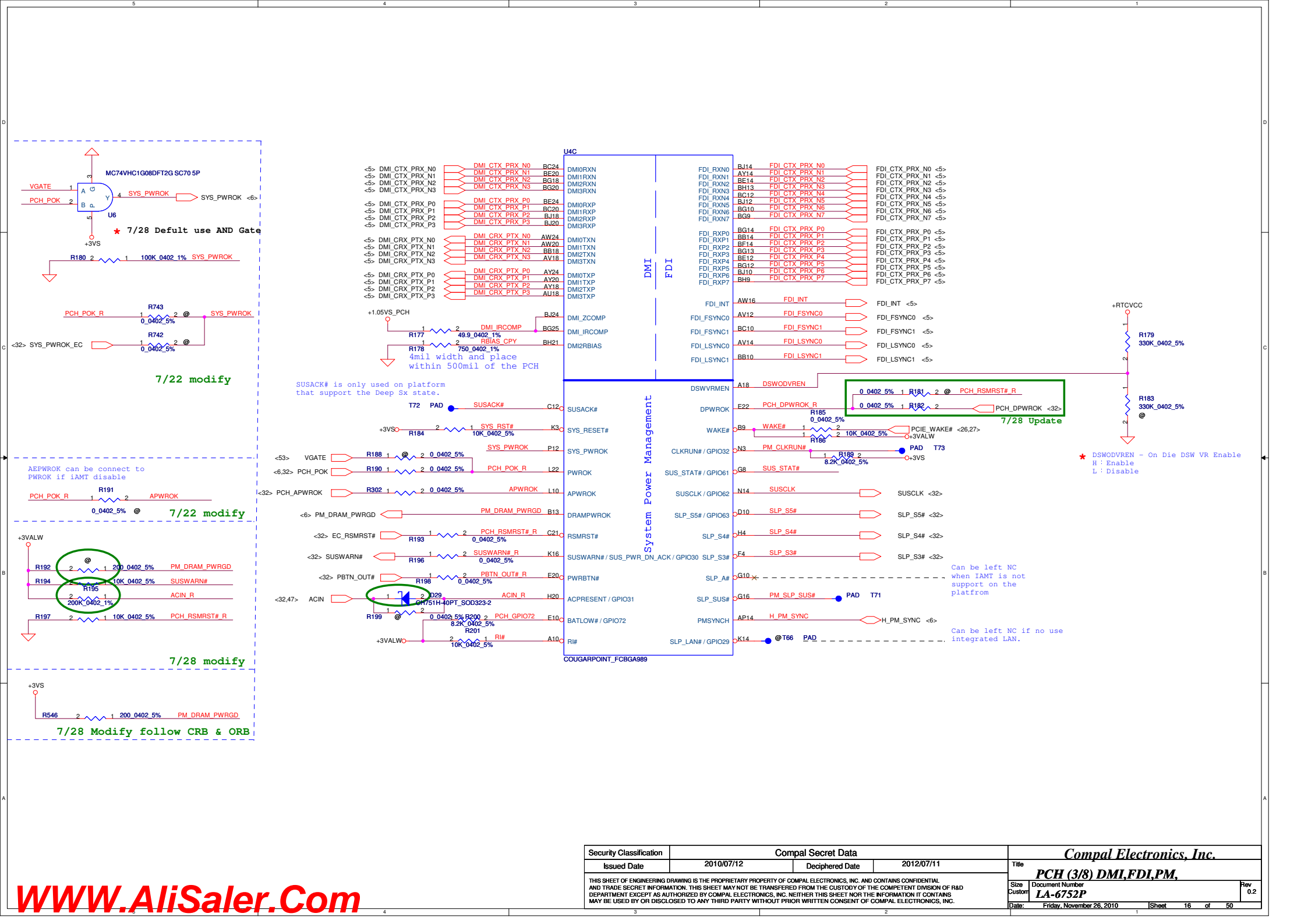
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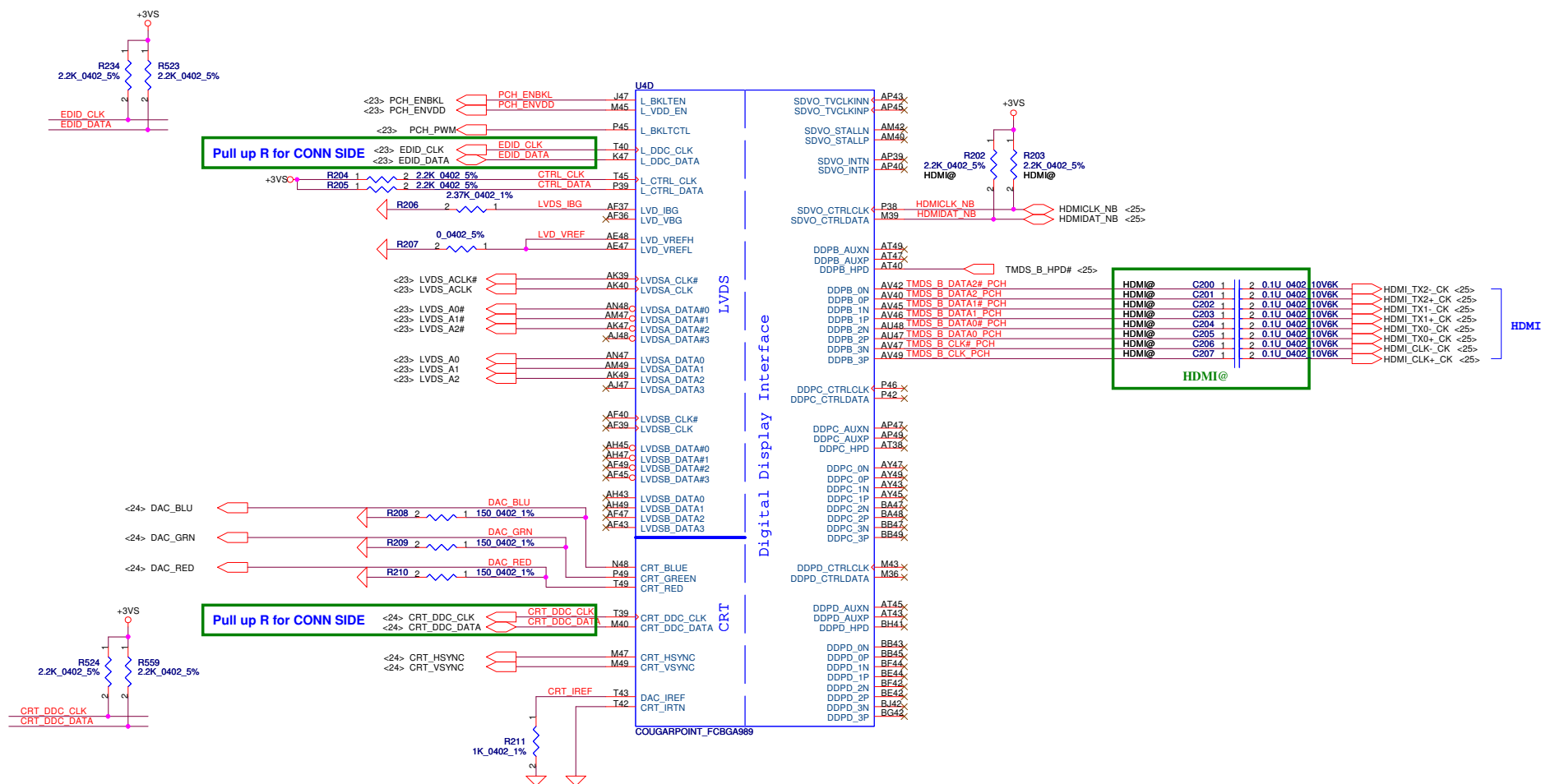
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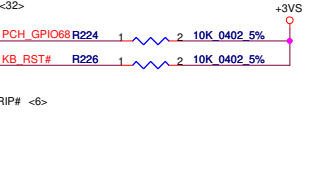
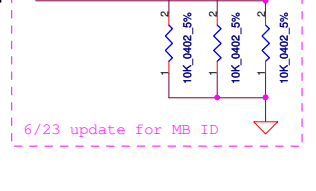
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				PCH (2/8) PCIE, SMBUS, CLK		
				Size		
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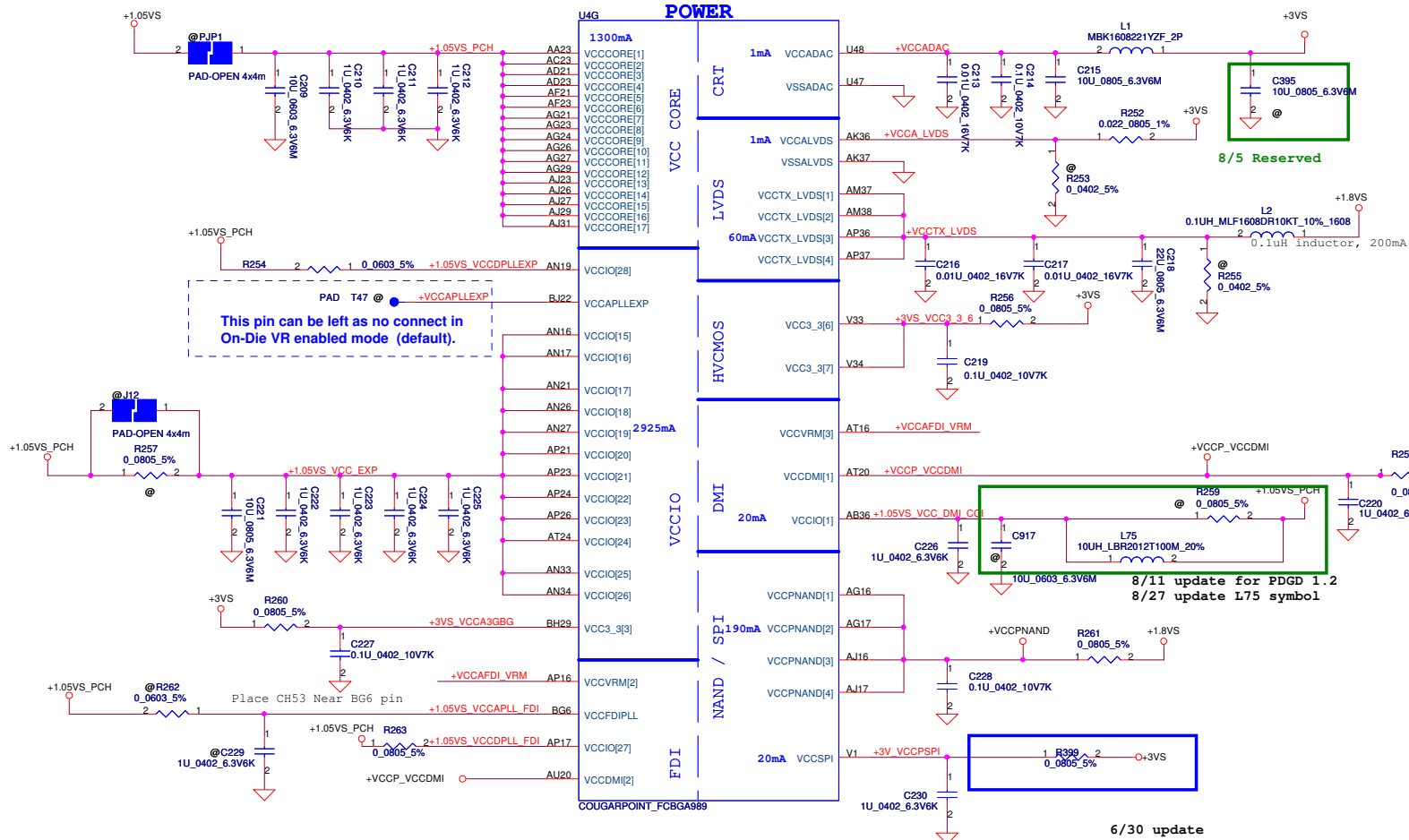


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								PCH (4/9) LVDS,CRT,DP,HDMI			
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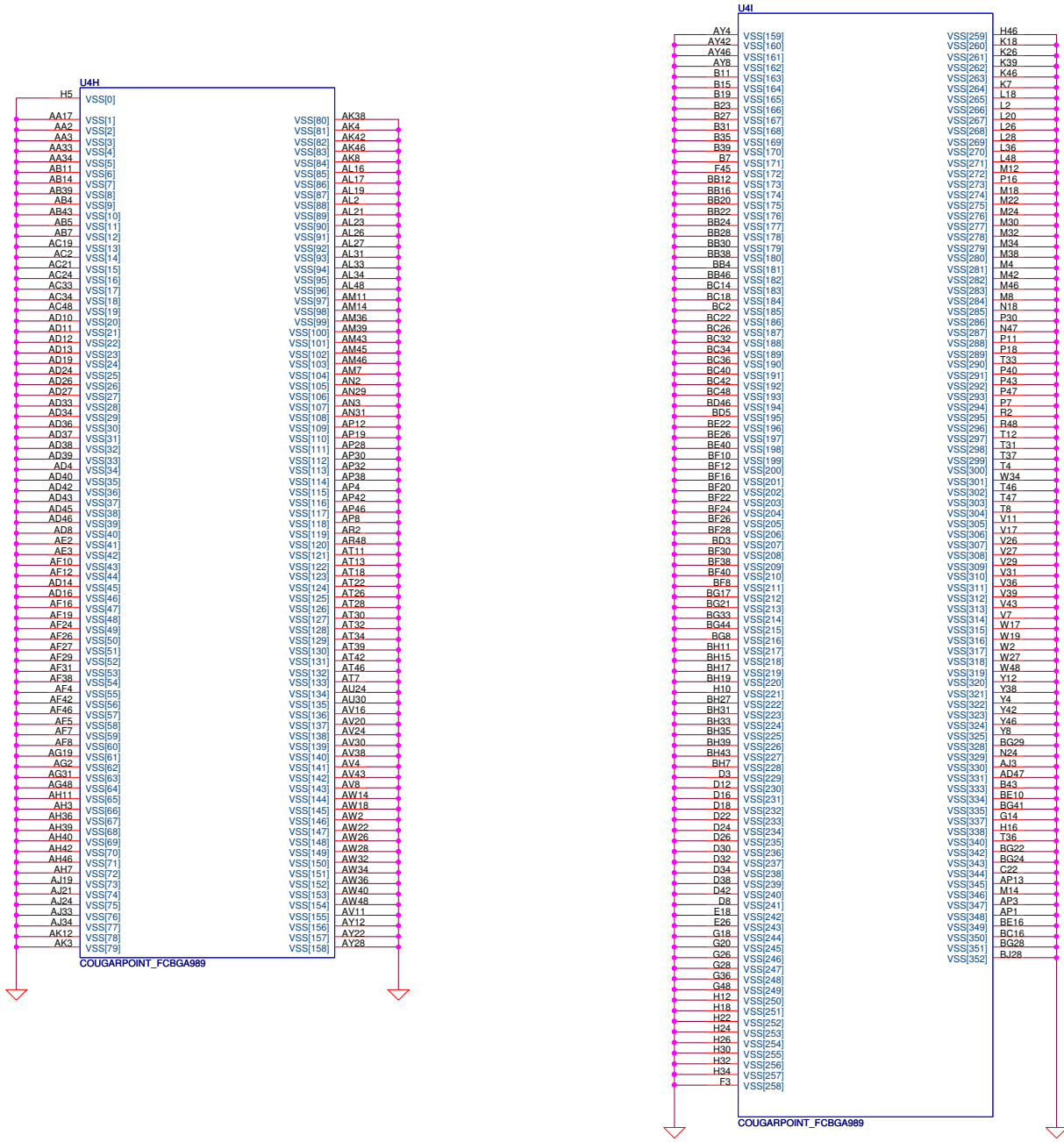
PCH Power Rail Table		
Voltage Rail	Voltage	SO Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.266
VccADAC	3.3	0.001
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.3
VccDMI	1.05	0.042
VccIO	1.05	2.925
VccASW	1.05	1.01
VccSPI	3.3	0.02
VccDSW	3.3	0.003
VccpNAND	1.8	0.19
VccRTC	3.3	6 uA
VccSus3_3	3.3	0.119
VccSusHDA	3.3 / 1.5	0.01
VccVRM	1.8 / 1.5	0.16
VccCLKDMI	1.05	0.02
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.06

Intel recommend stuff R265 and unstuff R266

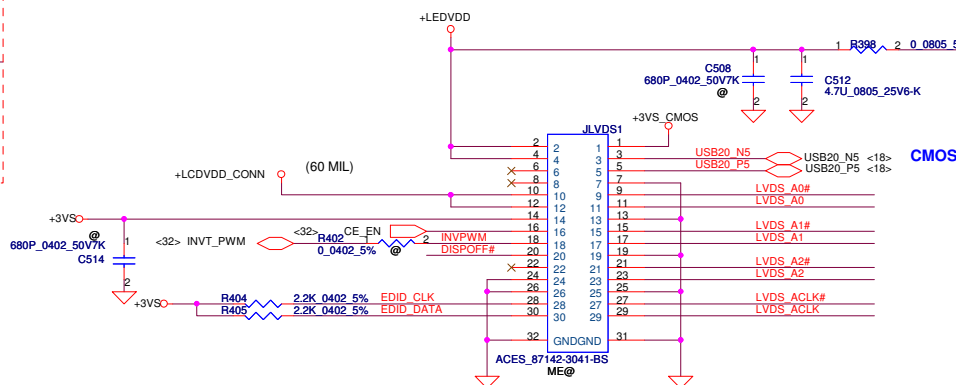
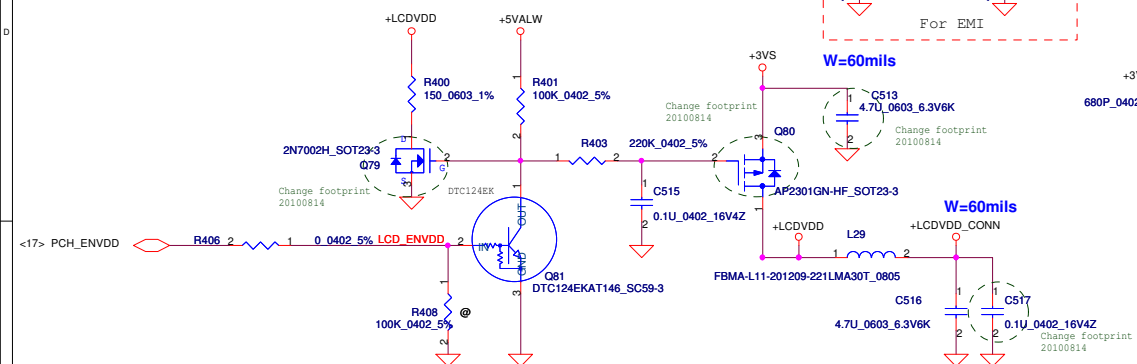
VCCVRM==>1.5V FOR MOBILE
VCCVRM==>1.8V FOR DESKTOP

VCCVRM = 160mA detail waiting for newest spec

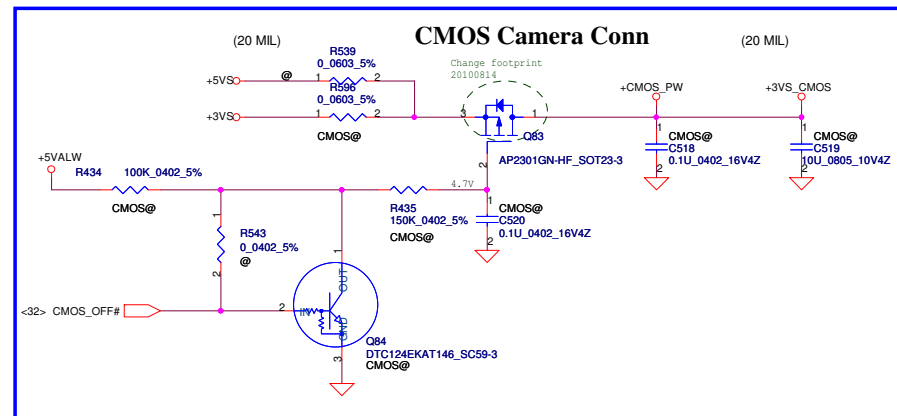
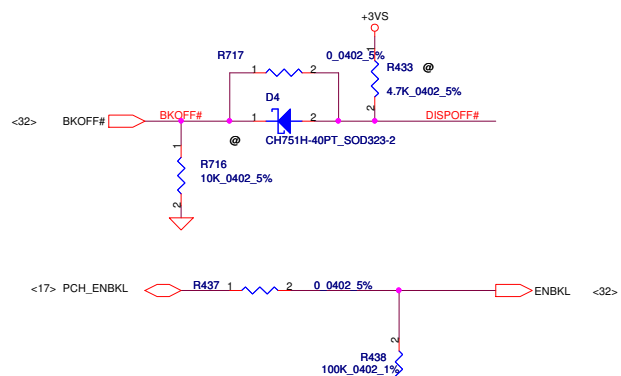
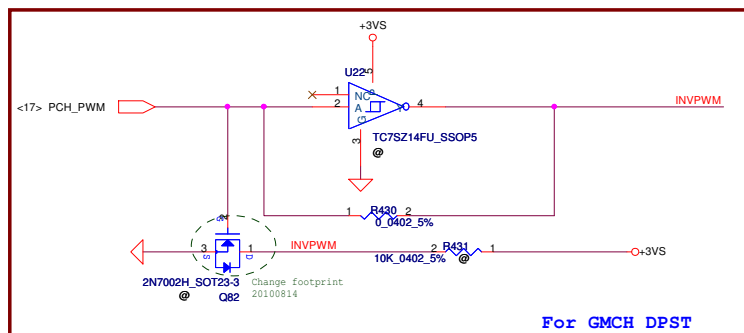
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				PCH (9/9) VSS		
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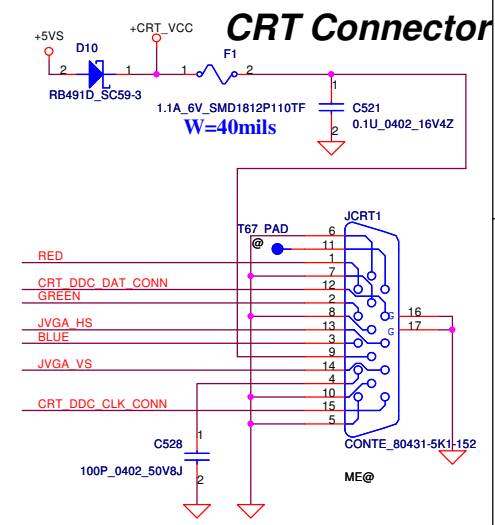
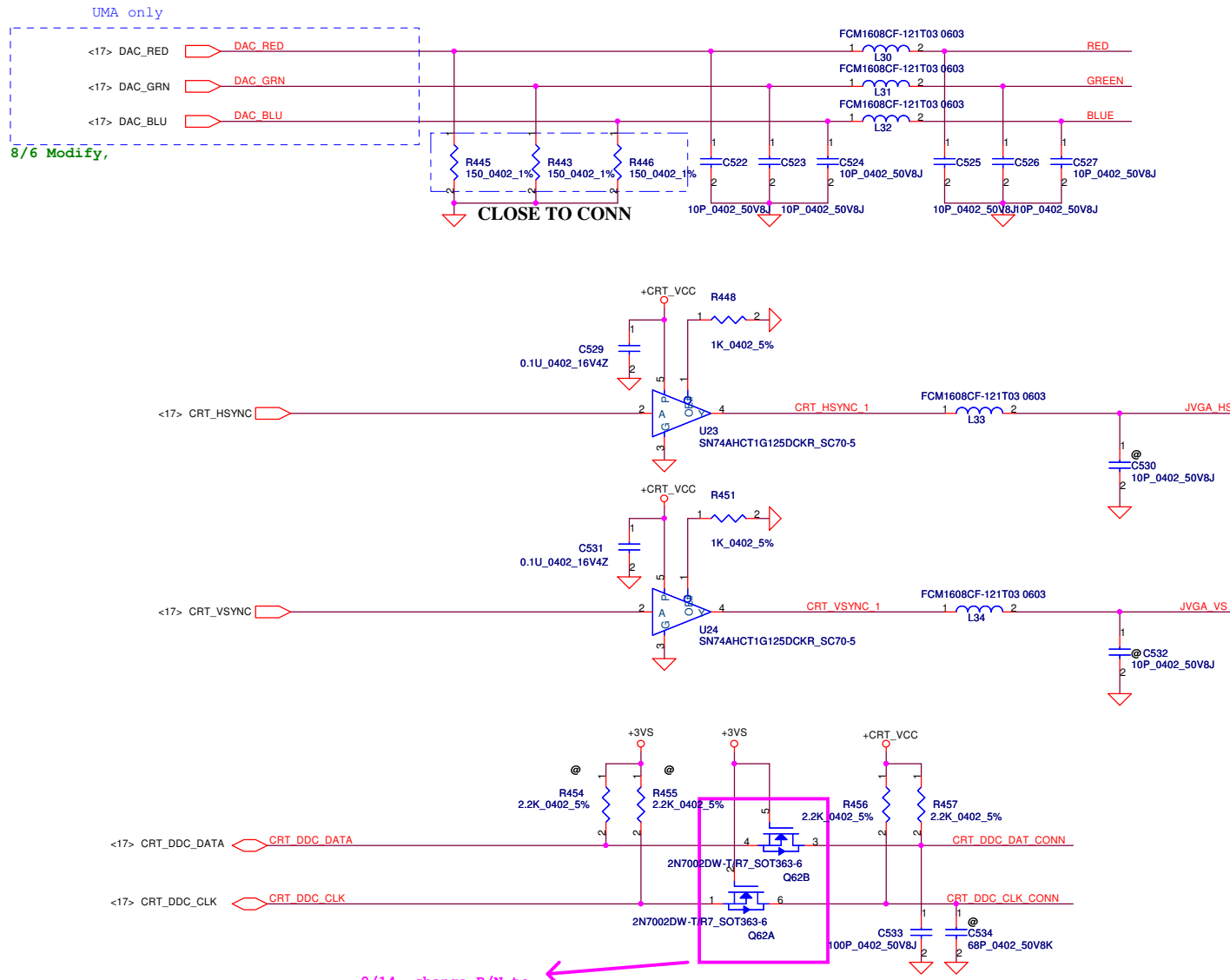
LCD POWER CIRCUIT



<17> EDID_CLK EDID_CLK
 <17> EDID_DATA EDID_DATA
 <17> LVDS_A0 LVDS_A0#
 <17> LVDS_A0# LVDS_A0#
 <17> LVDS_A1 LVDS_A1#
 <17> LVDS_A1# LVDS_A1#
 <17> LVDS_A2 LVDS_A2#
 <17> LVDS_A2# LVDS_A2#
 <17> LVDS_ACLK LVDS_ACLK#
 <17> LVDS_ACLK# LVDS_ACLK#

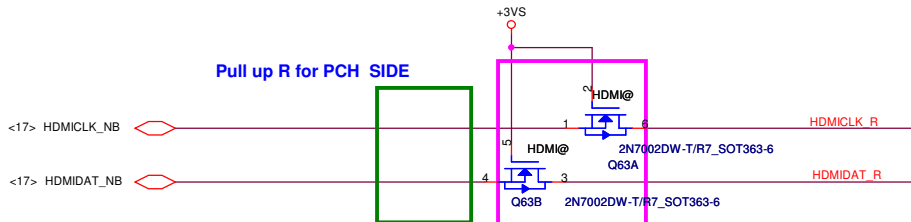
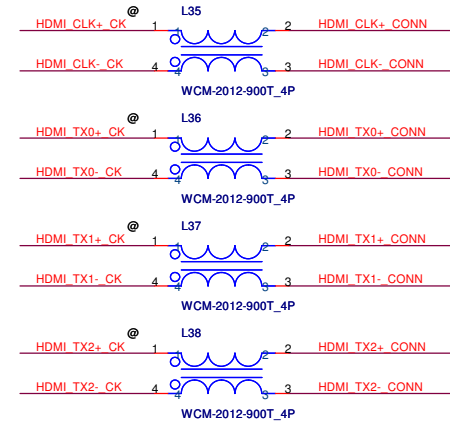
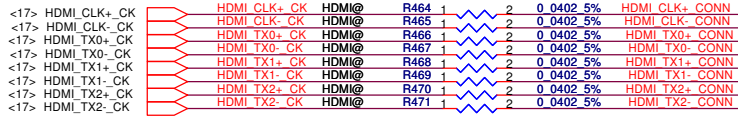
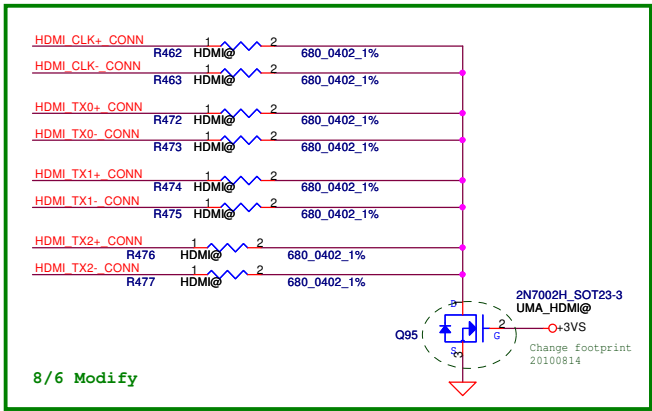


Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date				Deciphered Date				Title			
2010/07/12				2012/07/11				LVDS/CAMERA			
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								LA-6752P			
								Rev 0.2			
								Date: Friday, November 26, 2010			
								1 Sheet 23 of 50			

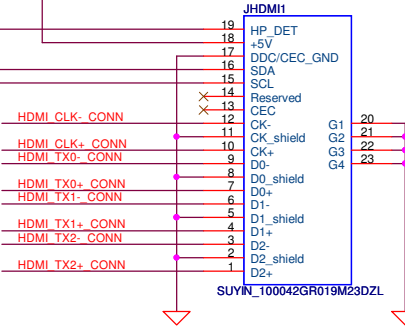
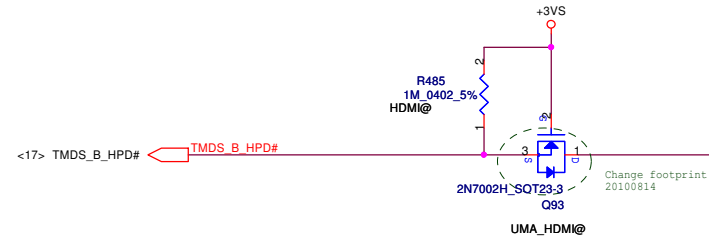
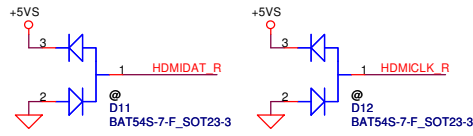
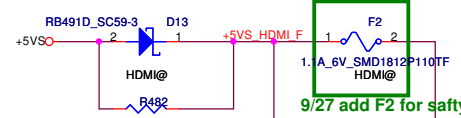


8/14 change P/N to
DMN6D0LDW-7_SOT363-6
(SB00000DH00)

Security Classification		Compal Secret Data		Title	
Issued Date	2010/07/12	Deciphered Date	2012/07/11	Compal Electronics, Inc.	
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Size	Custom	Document Number	LA-6752P		Rev 0.2
Date:	Friday, November 26, 2010	Sheet	24	of	50

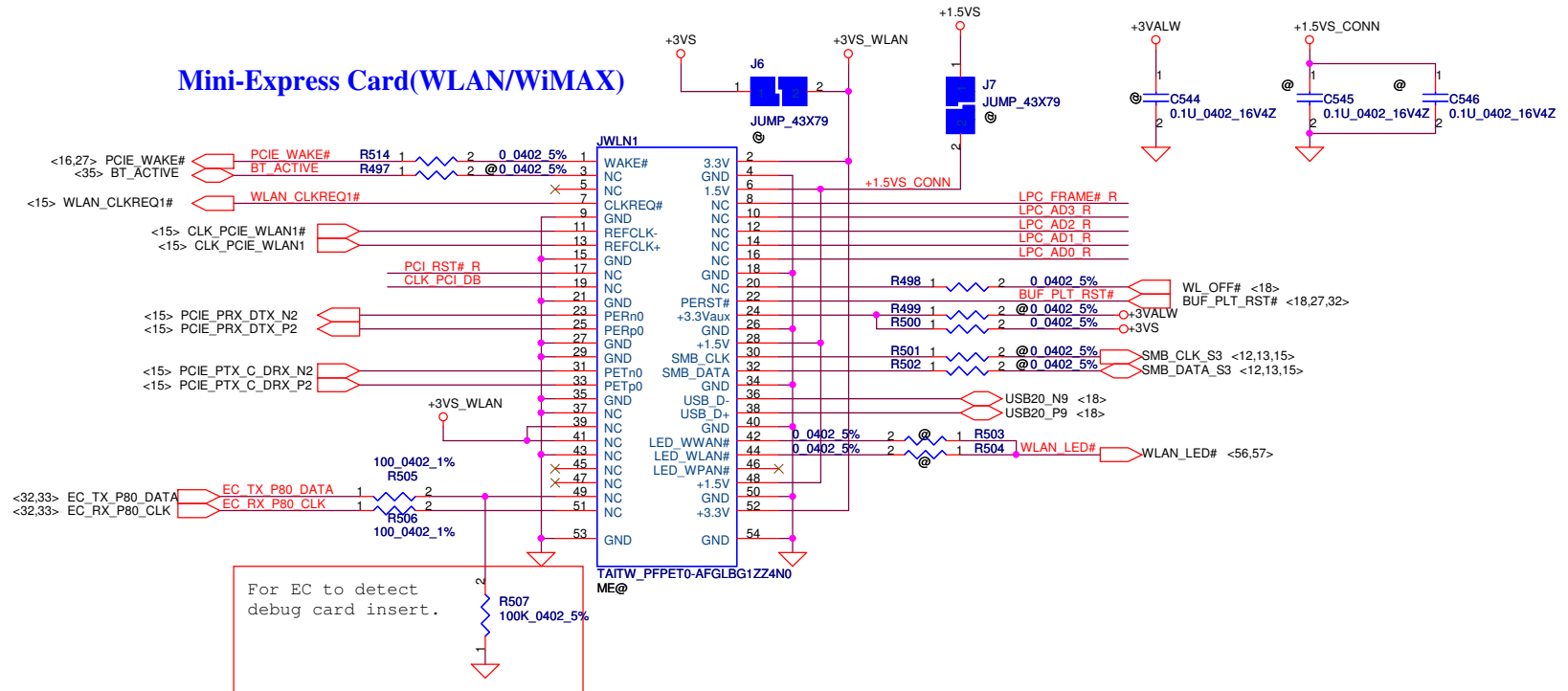


8/14 change P/N to DMN66D0LDW-7_SOT363-6 (SB00000DH00)



Security Classification		Compal Secret Data		Compal Electronics, Ltd.	
Issued Date	2010/07/12	Deciphered Date	2012/07/11	Title	HDMI CONN
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				Custom	LA-6752P
				Date	Friday, November 26, 2010
				Sheet	25 of 50
				Rev	0.2

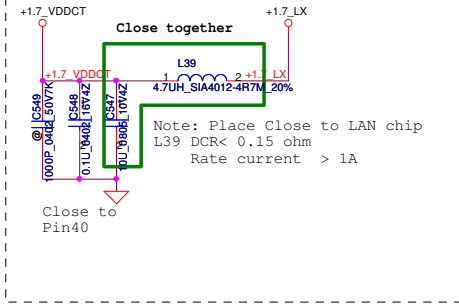
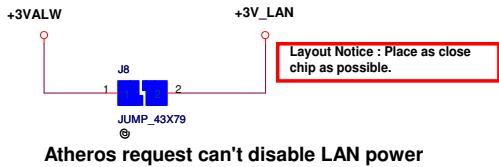
Mini-Express Card for WLAN/WiMAX(Half)



Reserve for SW mini-pcie debug card.
Series resistors closed to KBC side.

LPC_FRAME# R	R508	1	2	0.0402 5%	LPC_FRAME#	LPC_FRAME# <14,32>
LPC_AD3 R	R509	1	2	0.0402 5%	LPC_AD3	LPC_AD3 <14,32>
LPC_AD2 R	R510	1	2	0.0402 5%	LPC_AD2	LPC_AD2 <14,32>
LPC_AD1 R	R511	1	2	0.0402 5%	LPC_AD1	LPC_AD1 <14,32>
LPC_AD0 R	R512	1	2	0.0402 5%	LPC_AD0	LPC_AD0 <14,32>
PCI_RST# R	R513	1	2	0.0402 5%	BUF_PLT_RST#	BUF_PLT_RST#
CLK_PCI_DB					CLK_PCI_DB	CLK_PCI_DB <15>

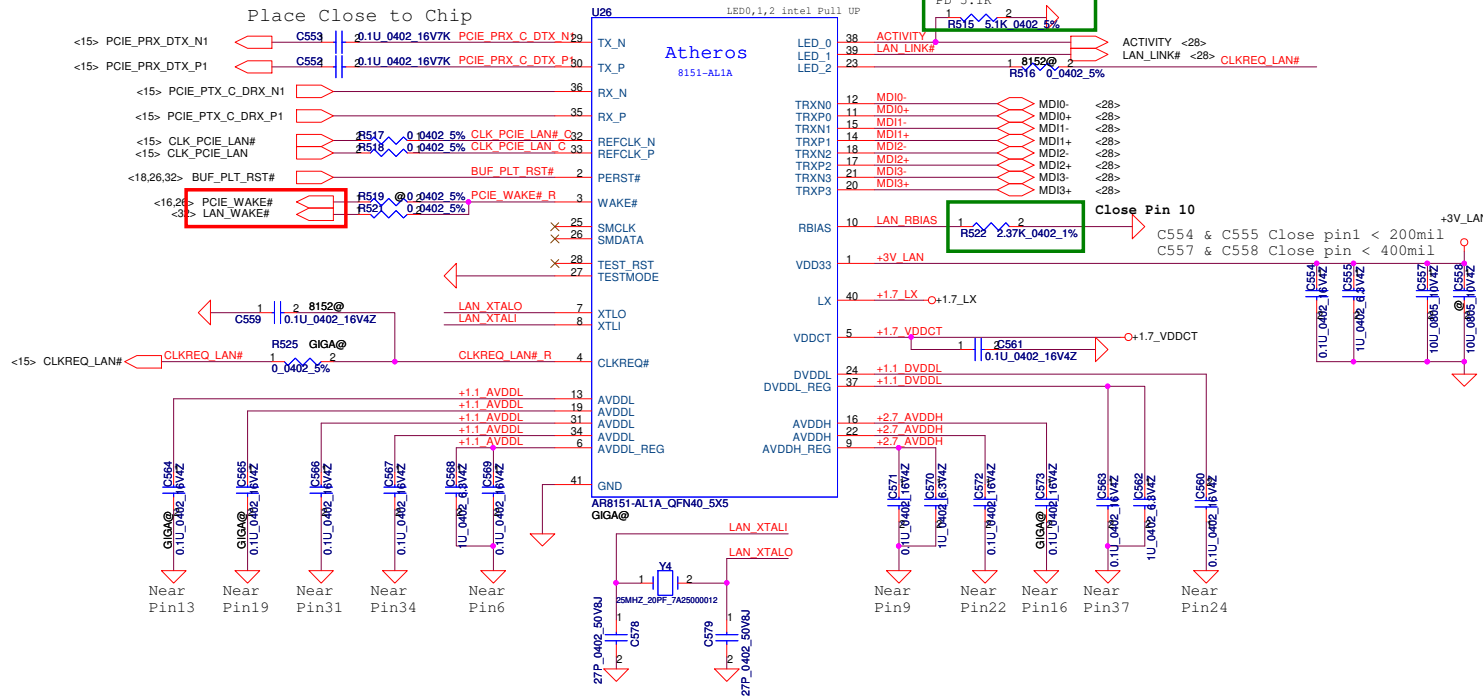
Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2010/07/12	Deciphered Date	2012/07/11	Title	
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				Size	Document Number
				LA-6752P	
				Date:	Friday, November 26, 2010
				Sheet	26 of 50
				Rev	0.2

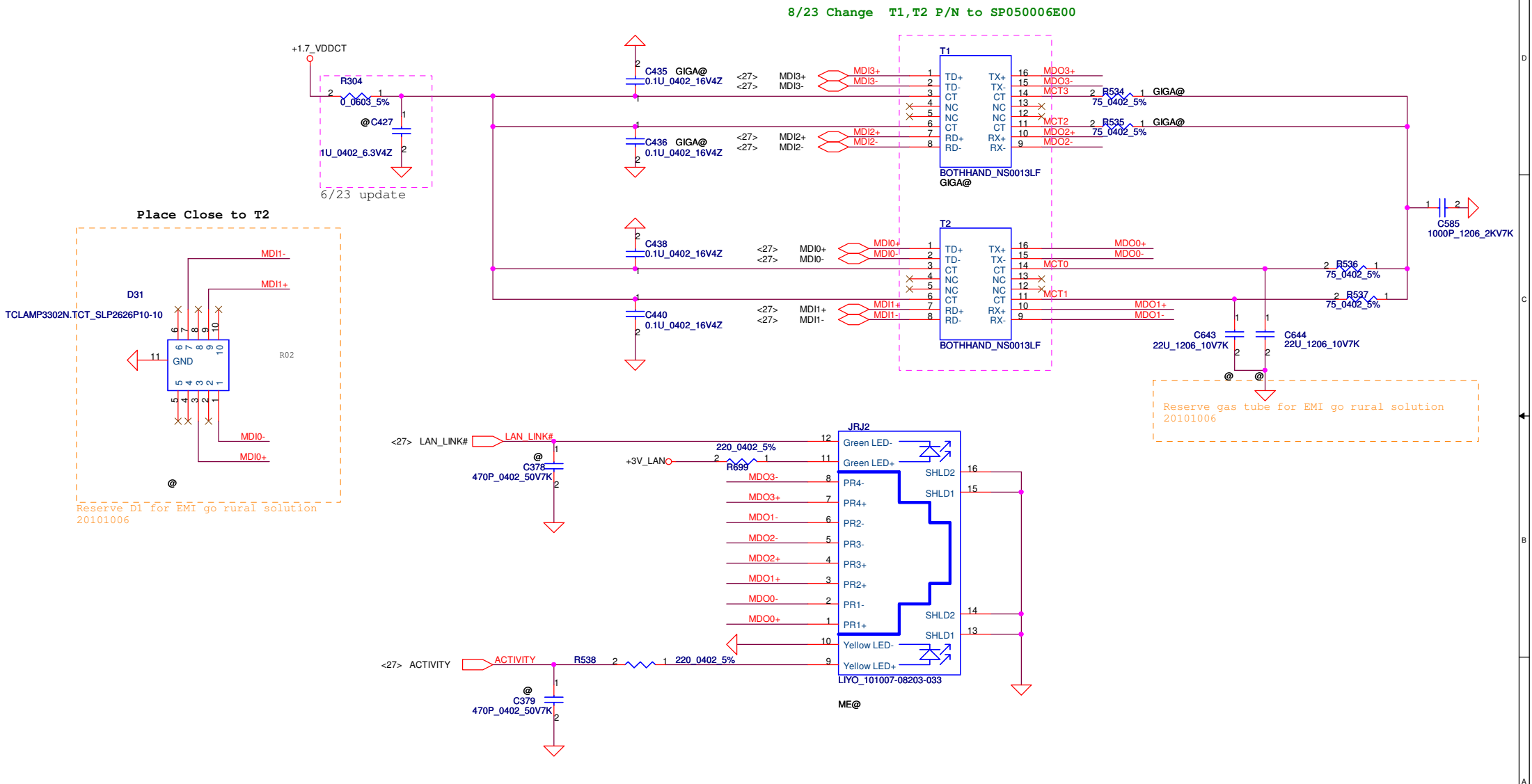


Power On strapping

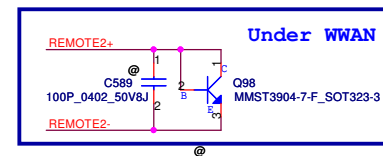
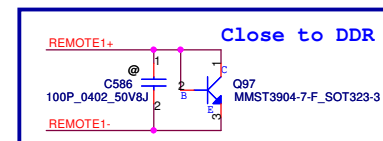
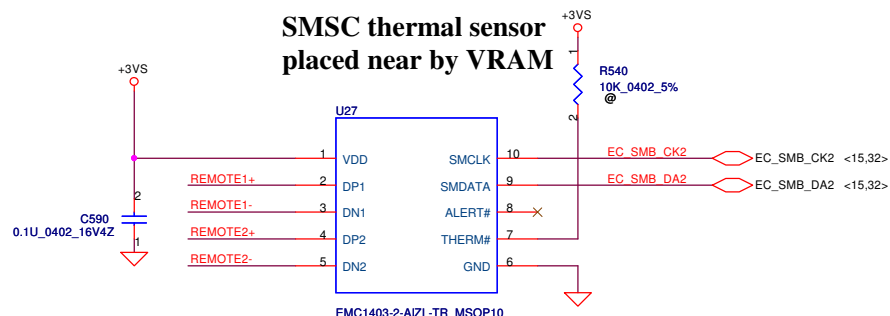
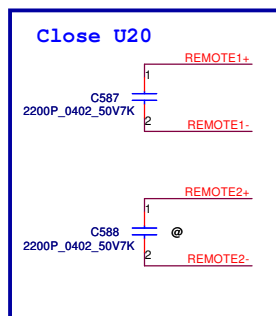
Pin	Description	Chip Default
LED0	H:Over Clock Enable L:Over Clock Disable *	H
LED2	H:SWR Switch mode regulator Select * AR8151 Pin23=LED2. AR8152, Pin23 is CLKREQ	--

U26 8152@
S IC AR8152-AL1E QFN 40P E-LAN CTRL

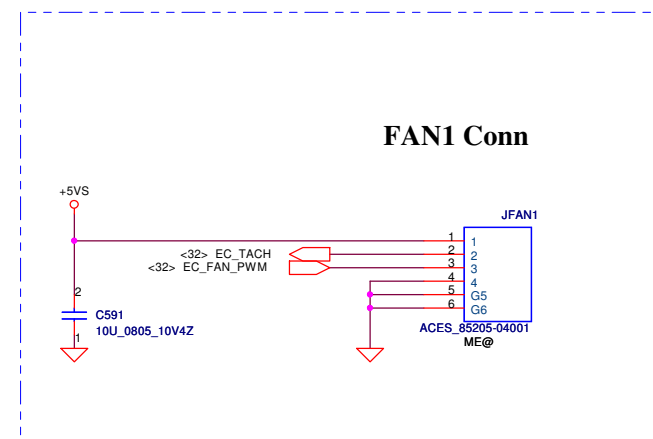




Security Classification		Compal Secret Data
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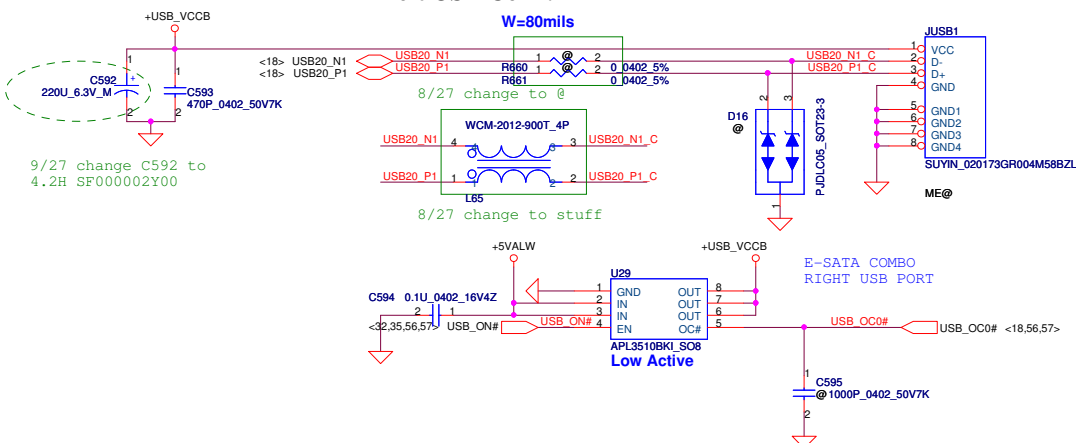


REMOTE1,2+/-:
Trace width/space:10/10 mil
Trace length:<8"

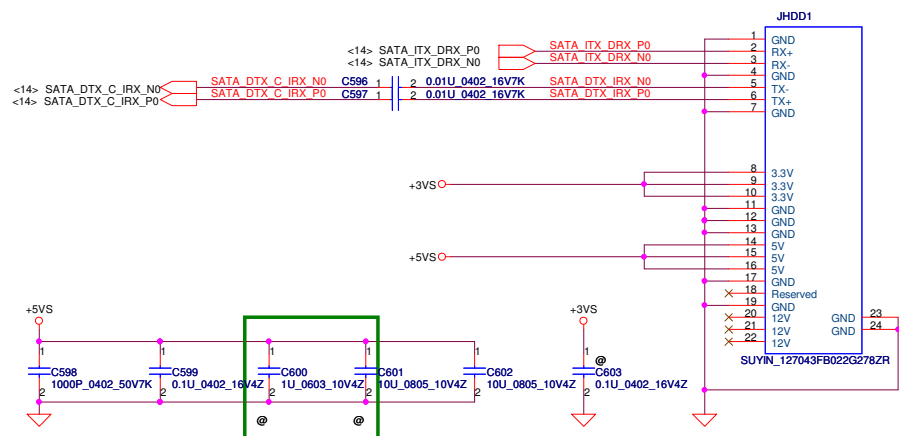


Security Classification		Compal Secret Data		Compal Electronics, Ltd.	
Issued Date	2010/07/12	Deciphered Date	2012/07/11	Title	EMC1403 Thermal sensor/FAN
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				Date: Friday, November 26, 2010	Sheet 29 of 50

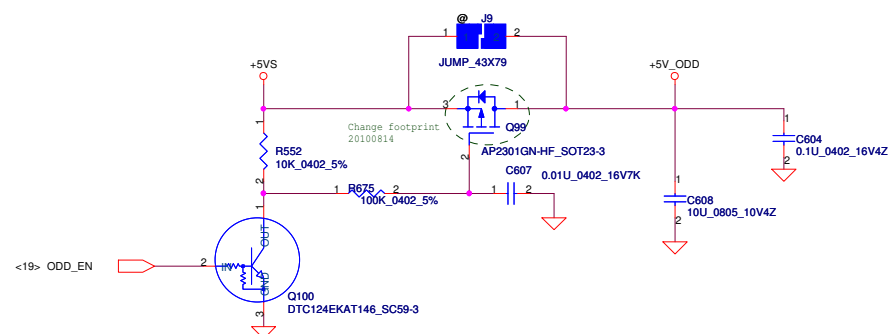
Left USB Conn.



SATA HDD Conn.



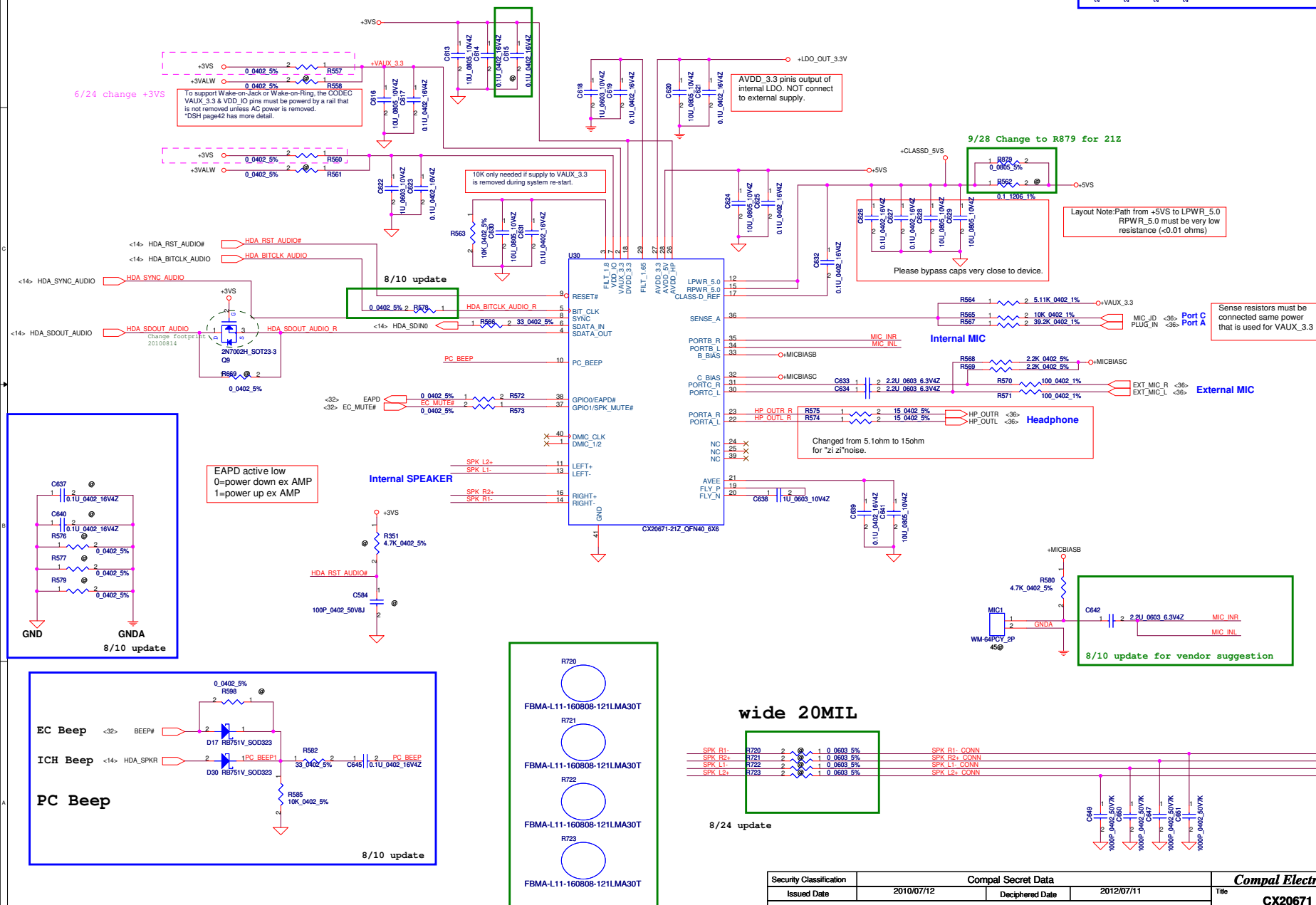
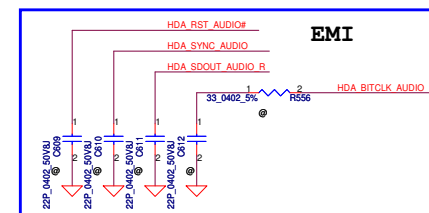
ODD Power Control



Security Classification		Compal Secret Data		Title	
Issued Date	2010/07/12	Deciphered Date	2012/07/11	Compal Electronics, Inc.	
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				Size B	Rev 0.2
Date: Friday, November 26, 2010		Sheet 30 of 50		LA-6752P	

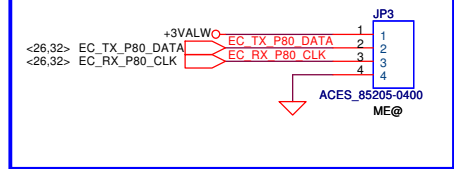
CK20671
High Definition Audio Codec SoC
With Integrated Class-D Stereo
Amplifier.
An integrated 5 V to 3.3 V Low-dropout
voltage regulator (LDO).
An integrated 3.3 V to 1.8V Low-dropout
voltage regulator (LDO).

9/27 Update U30 P/N to SA00003K410



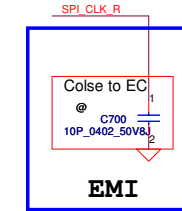
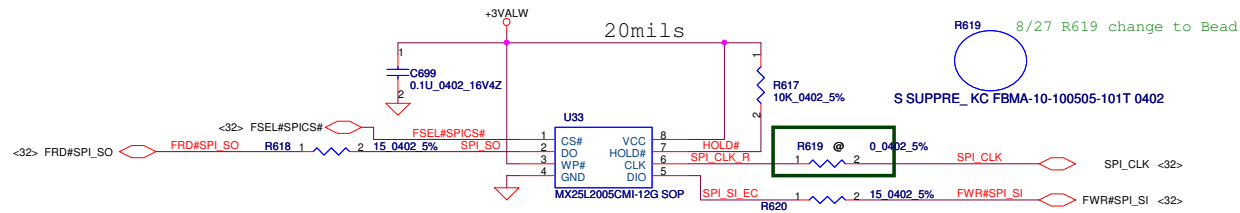
Security Classification		Compal Secret Data		Compal Electronics, Ltd.	
Issued Date		Deciphered Date		Title	
2010/07/12		2012/07/11		CX20671 Codec	
Size		Document Number		LA-6752P	
Date: Friday, November 26, 2010		Sheet		31 of 50	

EC DEBUG PORT

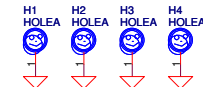


Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2010/07/12	Deciphered Date	2012/07/11	Title	
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				Size B	Document Number
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				Rev 0.2	

FOR EC 128KB SPI ROM
(150mil PACKAGE)
SA00003FL10
SA00003JD00



H_3P8



H_3P3



H_3P0x4P5N



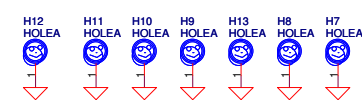
H_3P0N



H_6P0

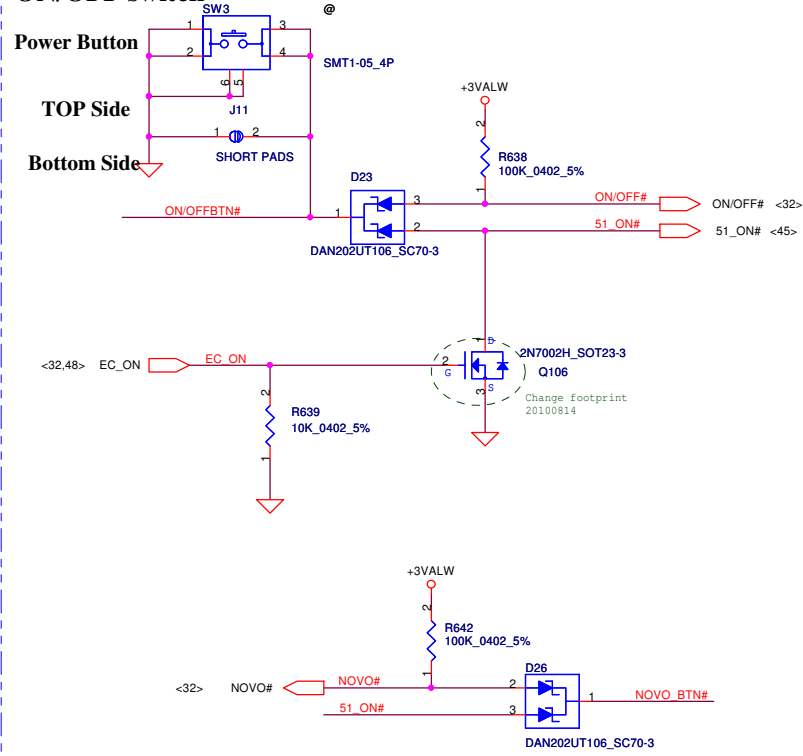


H_2P8

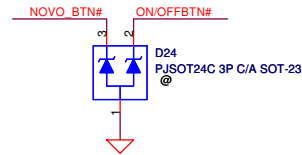
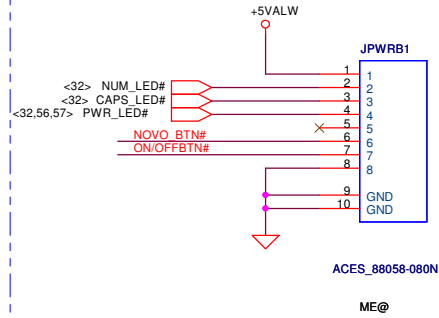


Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2010/07/12	Deciphered Date	2012/07/11	Title	LED/EC SPI ROM
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				Rev	0.2

ON/OFF switch

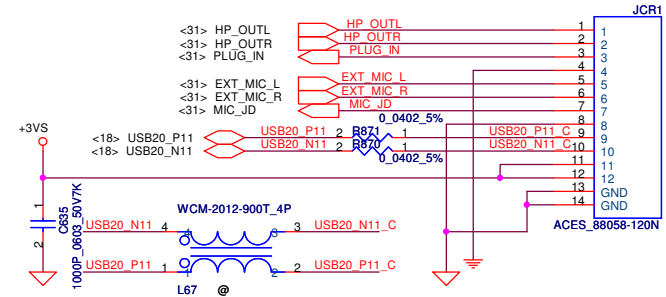


Power Bottom Board Conn. 8pin



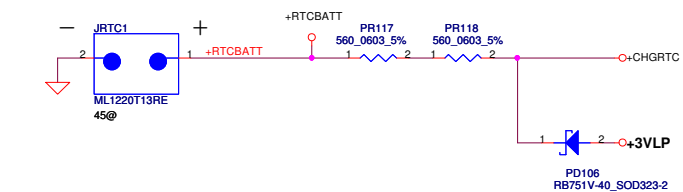
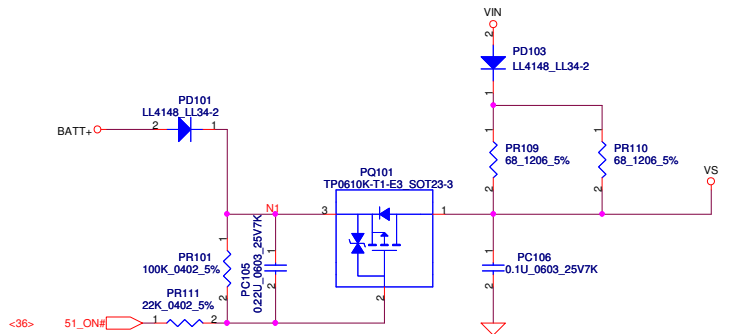
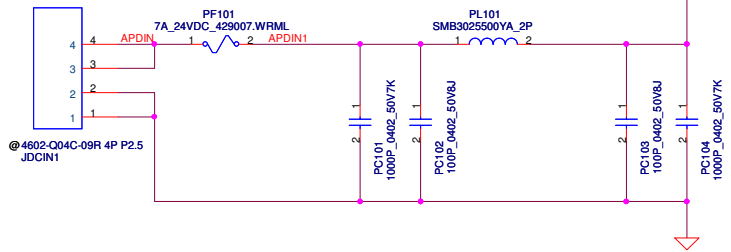
EMI REQUEST 1ST = SCA000000E00
2ST = SCA000000R00

Card Reader/Audio Jack SB CONN

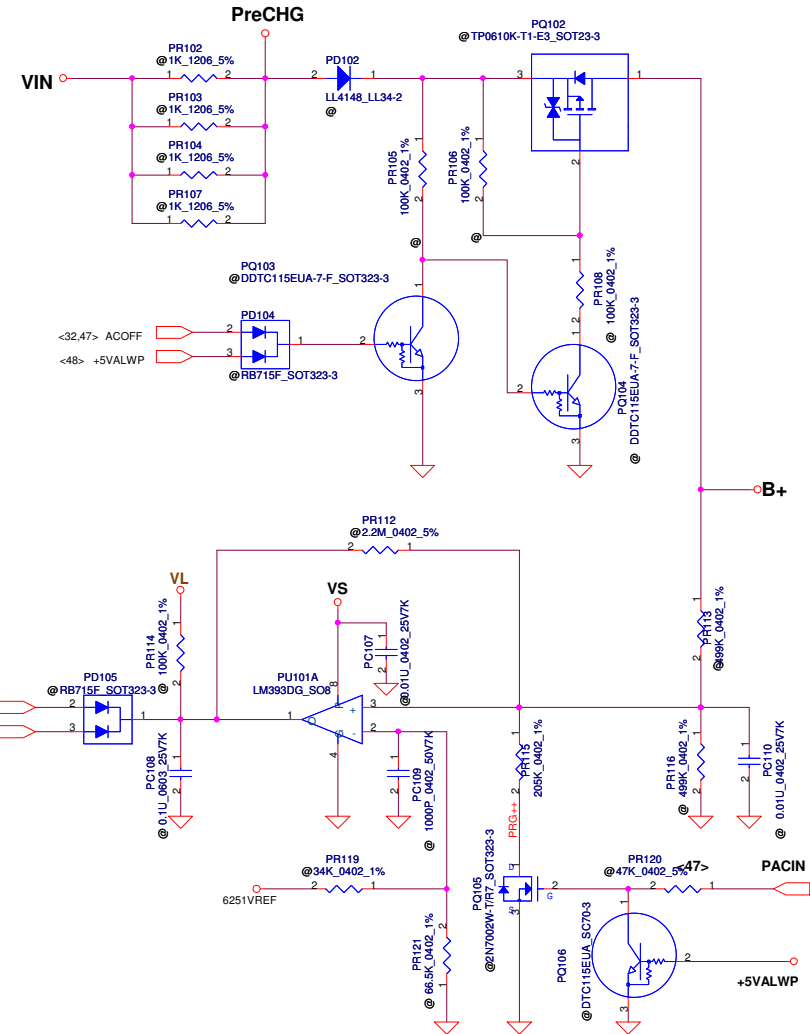


Security Classification	Compal Secret Data		Compal Electronics, Ltd.	
Issued Date	2010/07/12	Deciphered Date	2012/07/11	Title
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DC030006J00



Precharge detector
15.97V/14.84V FOR
ADAPTOR



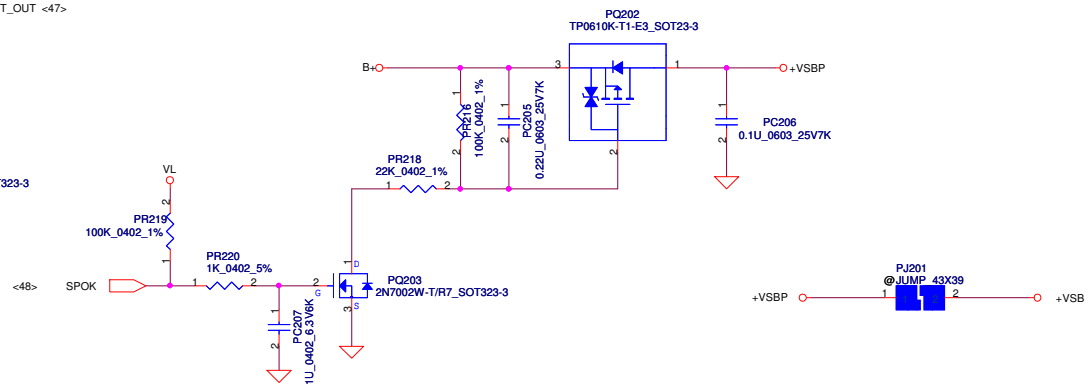
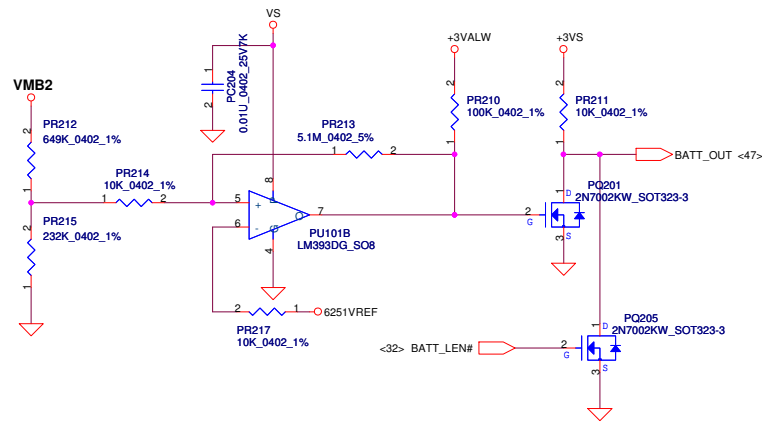
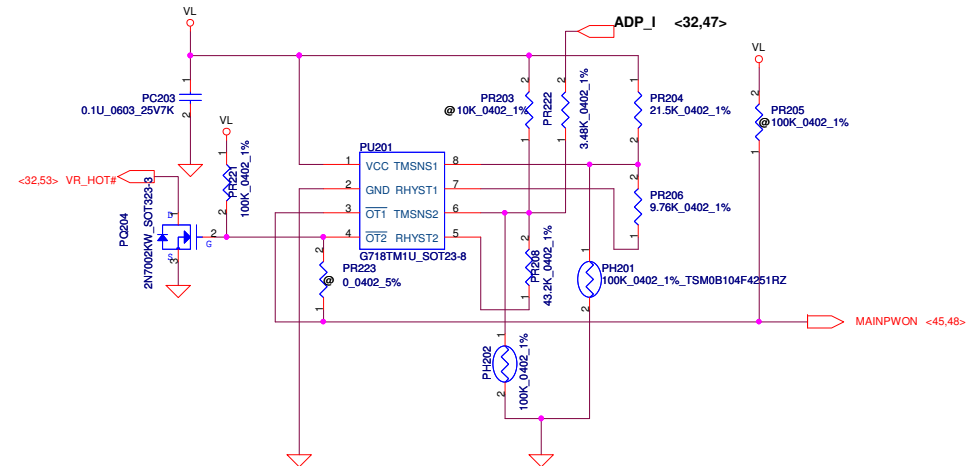
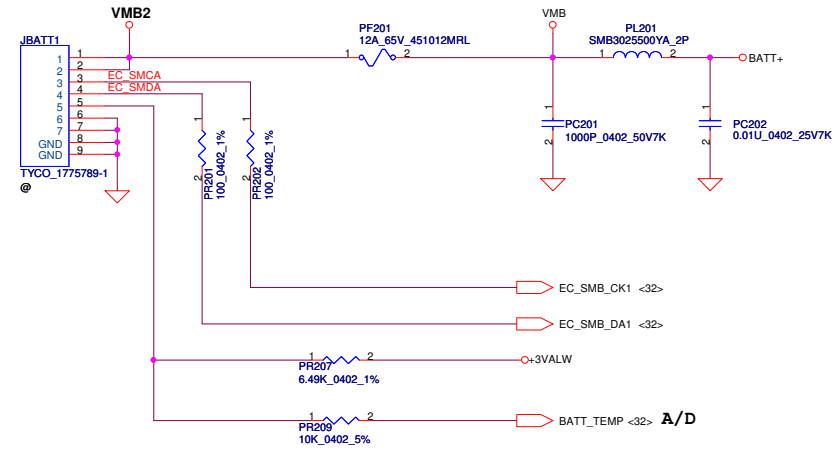
ACIN

Precharge detector			
Min.	typ.	Max.	
L-->H	14.991V	15.381V	15.782V
H-->L	13.860V	14.247V	14.621V

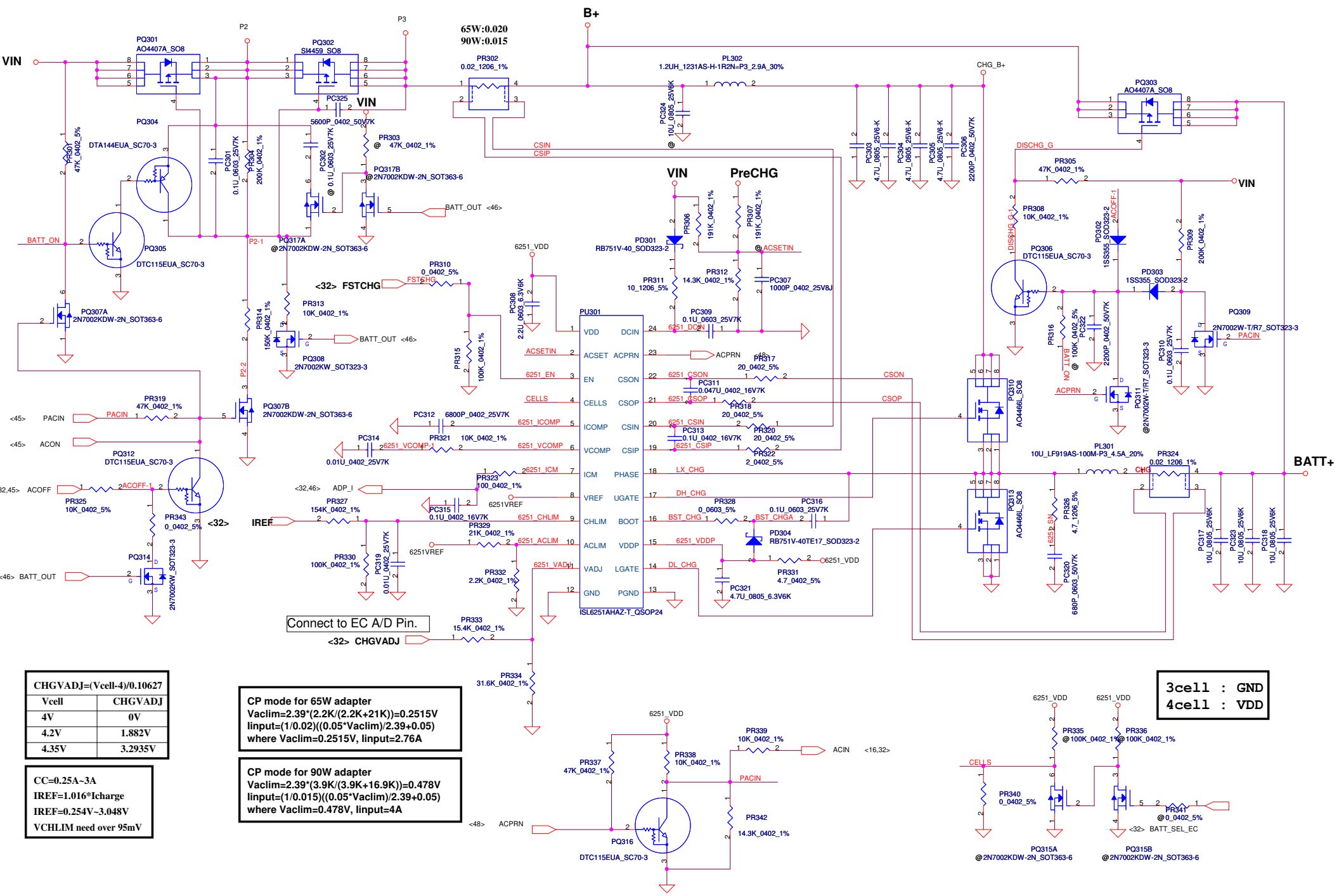
BATT ONLY

Precharge detector			
Min.	typ.	Max.	
L-->H	7.196V	7.349V	7.505V
H-->L	6.138V	6.214V	6.056V

Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2010/01/25	Deciphered Date	2010/12/31	Title PWR DCIN / Vin Detector /Pre-charge	
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				Date Friday, November 26, 2010	Rev 0.1
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Connect to EC A/D Pin.

<32> CHGVADJ

CP mode for 65W adapter
 $V_{acim}=2.39 \times (2.2K / (2.2K + 21K)) = 0.2515V$
 $Input = (1/0.02) \times ((0.05 \times V_{acim}) / (2.39 + 0.05))$
where $V_{acim}=0.2515V$, $Input=2.76A$

CP mode for 90W adapter
 $V_{acim}=2.39 \times (3.9K / (3.9K + 16.9K)) = 0.478V$
 $Input = (1/0.015) \times ((0.05 \times V_{acim}) / (2.39 + 0.05))$
where $V_{acim}=0.478V$, $Input=4A$

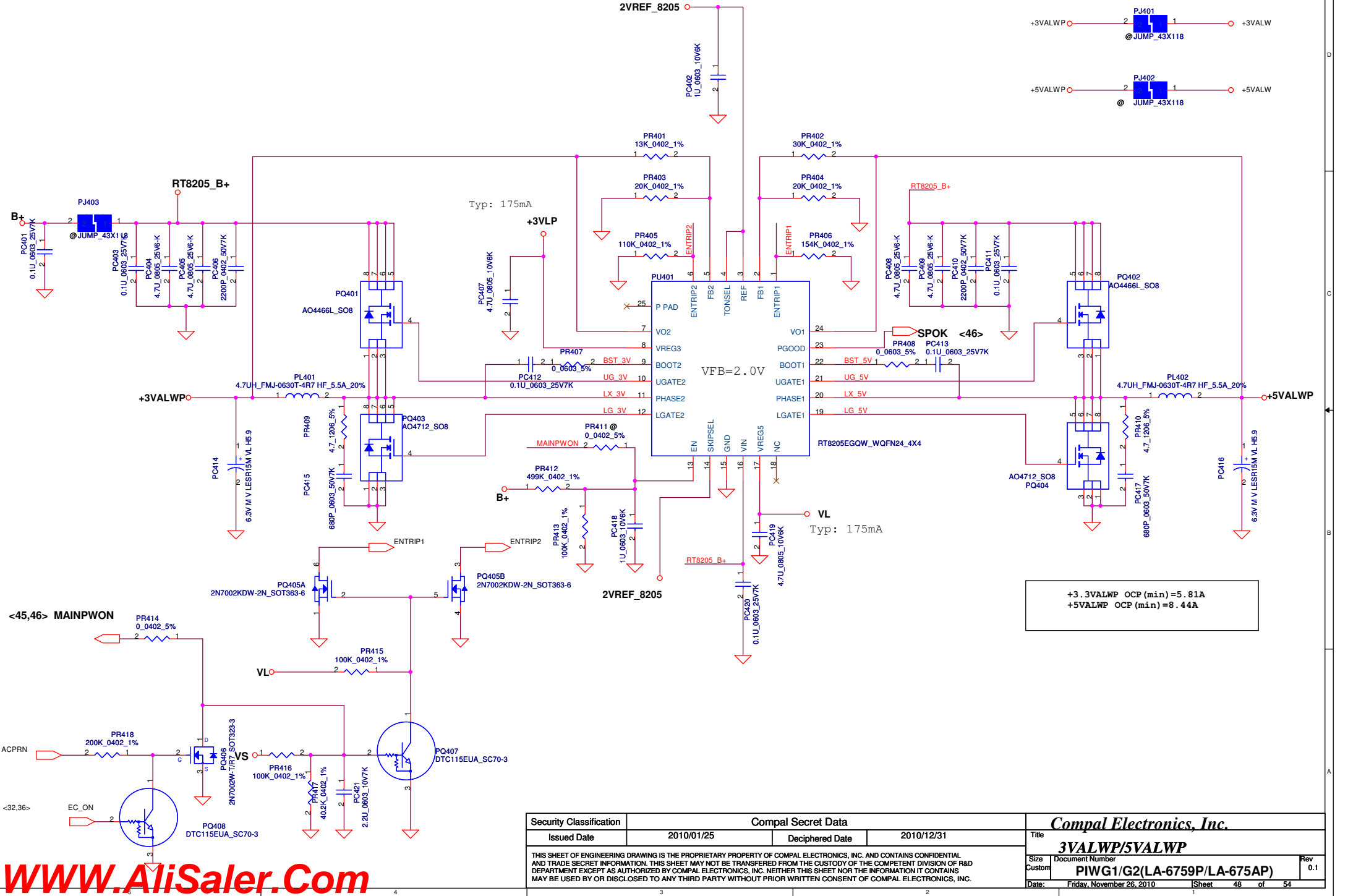
CHGVADJ=(Vcell-4)/0.10627	
Vcell	CHGVADJ
4V	0V
4.2V	1.882V
4.35V	3.2935V

CC=0.25A~3A
IREF=1.016*Icharge
IREF=0.254V~3.048V
VCHLIM need over 95mV

3cell : GND
4cell : VDD

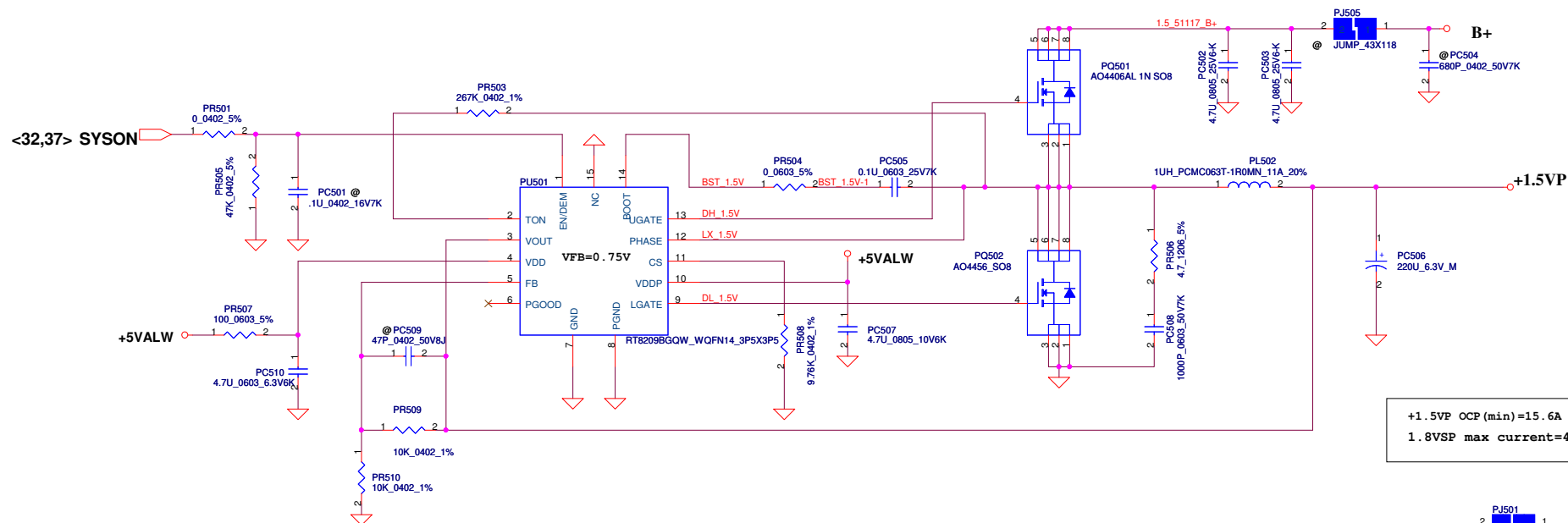
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2010/01/13	Deciphered Date	2011/01/13	Title	
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					PIWG1/G2(LA-6759P/LA-675AP)
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				Friday, November 26, 2010	0.2
				Sheet	47 of 54

Note:
Use TPS51125 IC can remove RTC refernece LDO
Use TPS51427 IC must keep RTC refernece LDO

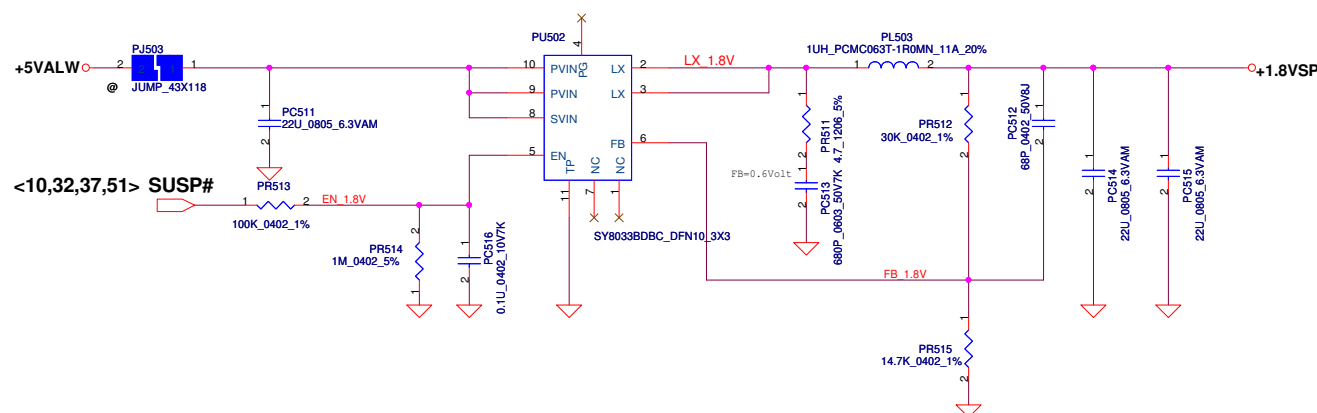
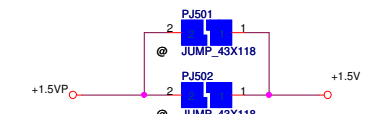


Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2010/01/25	Deciphered Date	2010/12/31	Title	3VALWP/5VALWP
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				Date	Friday, November 26, 2010
				Sheet	48 of 54

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+1.5VP OCP (min)=15.6A
1.8VSP max current=4A

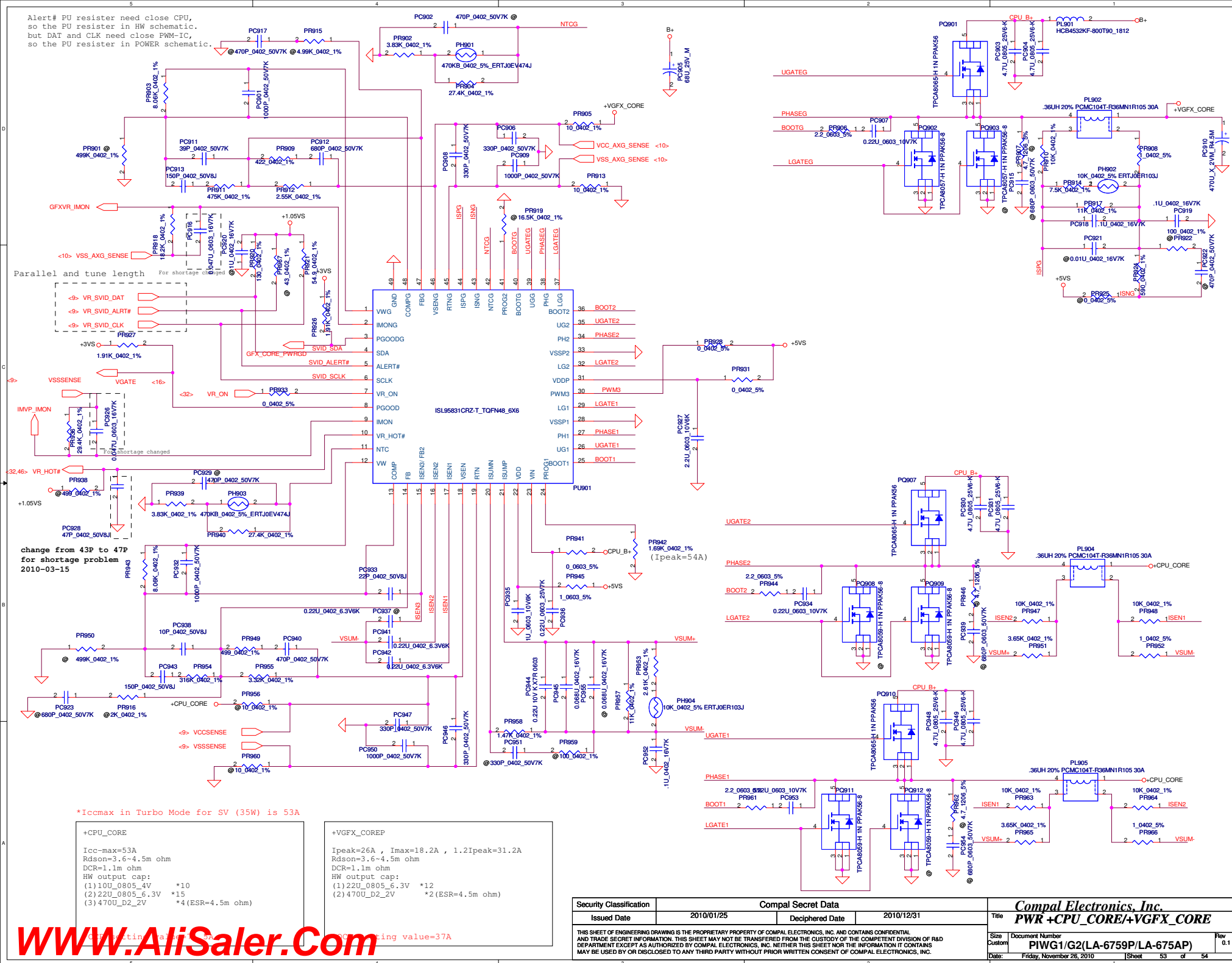


Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2010/01/25	Deciphered Date	2010/12/31	Title	
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Size		Document Number		Rev	
Custom		PIWG1/G2(LA-6759P/LA-675AP)		0.1	
Date:		Friday, November 26, 2010		Sheet 49 of 54	





Alert# PU resistor need close CPU,
so the PU resistor in HW schematic.
but DAT and CLK need close PWM-IC,
so the PU resistor in POWER schematic.



Parallel and tune length
For shortage changed

change from 43P to 47P
for shortage problem
2010-03-15

*Iccmax in Turbo Mode for SV (35W) is 53A

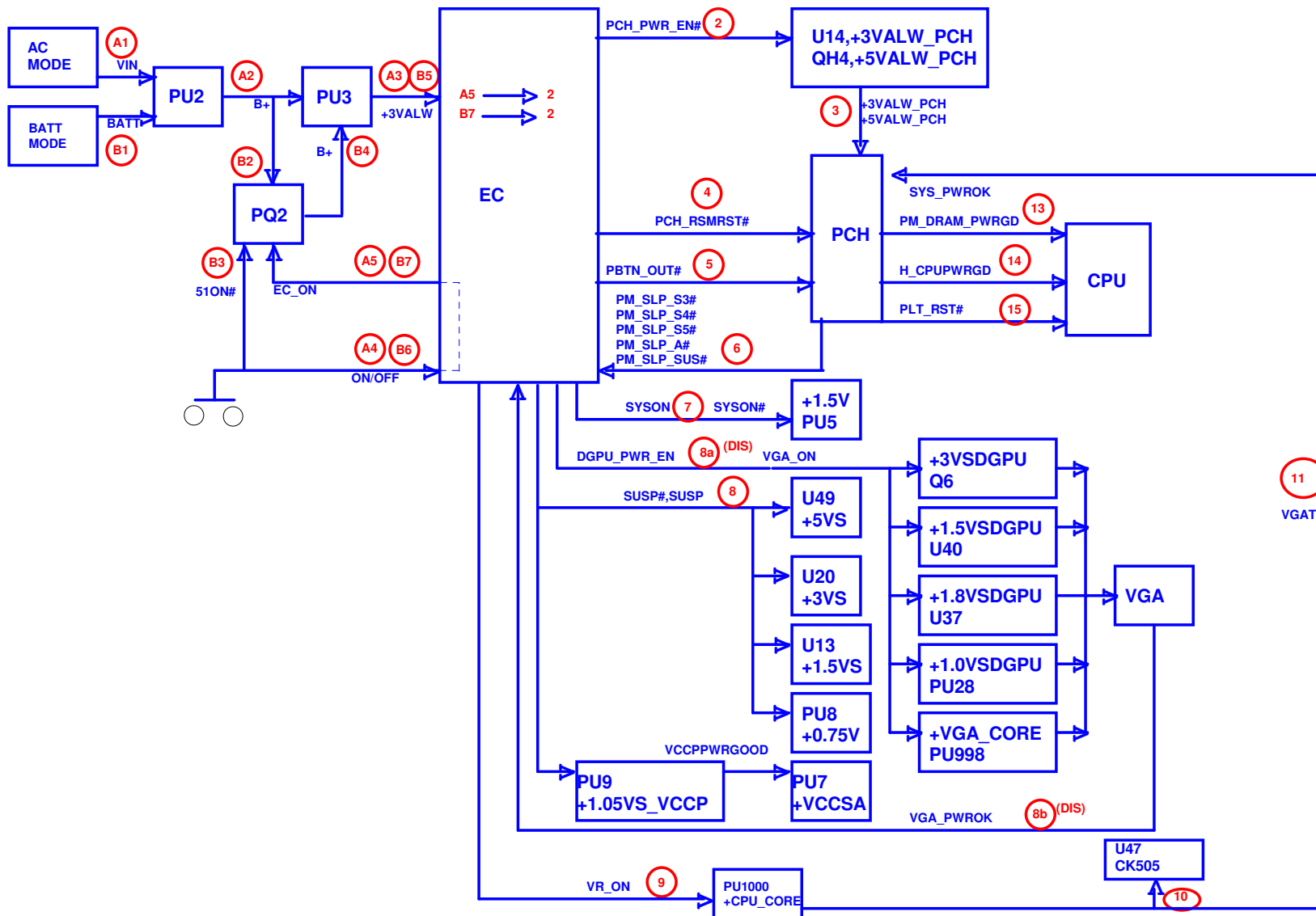
+CPU_CORE
Icc-max=53A
Rds-on=3.6~4.5m ohm
DCR=1.1m ohm
HW output cap:
(1) 10U_0805_4V *10
(2) 22U_0805_6.3V *15
(3) 470U_D2_2V *4 (ESR=4.5m ohm)

+VGFX_COREP
Ipeak=26A, Imax=18.2A, 1.2Ipeak=31.2A
Rds-on=3.6~4.5m ohm
DCR=1.1m ohm
HW output cap:
(1) 22U_0805_6.3V *12
(2) 470U_D2_2V *2 (ESR=4.5m ohm)

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Issued Date	2010/01/25	Deciphered Date	2010/12/31	Title PWR +CPU_CORE/+VGFX_CORE	
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				Custom	PWVG1/G2(LA-6759P/LA-675AP)
				Date:	Friday, November 26, 2010

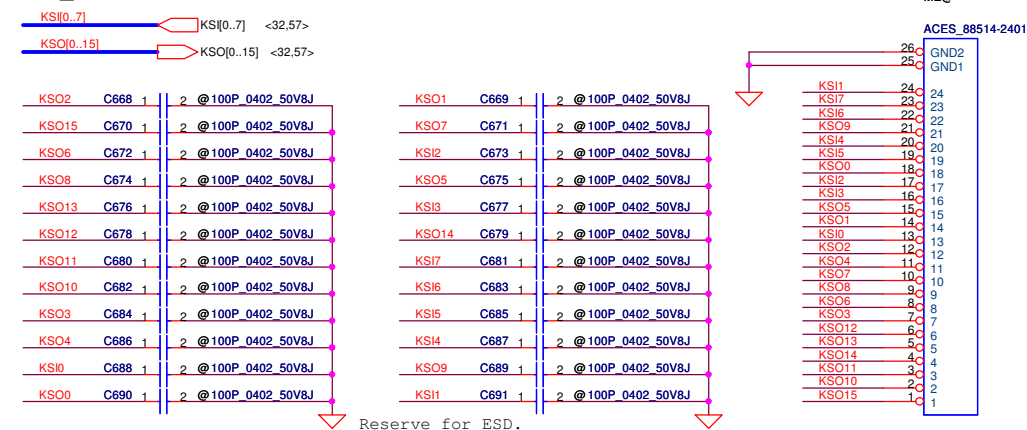
Item	Reason for change	PG#	Modify List	Date	Phase
1					
2					
3					
4					
5					
6					
7					
8					
9					
10					
11					
12					
13					
14					
15					
16					
17					

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				Size	Document Number	Rev
				Custom	PIWG1/G2(LA-6759P/LA-675AP)	0.1
Date:				Friday, November 26, 2010	Sheet 54 of 54	

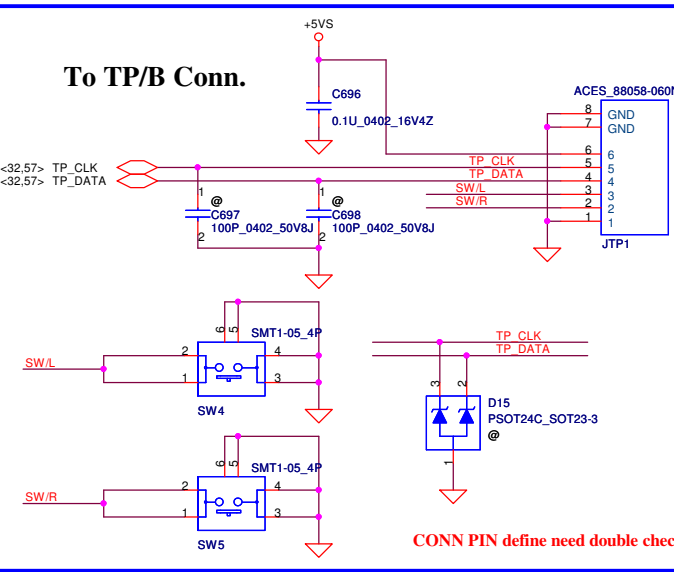


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Size	Custom	Document Number	LA-6752P	Rev	0.2
Date:	Friday, November 26, 2010	Sheet	55	of	60

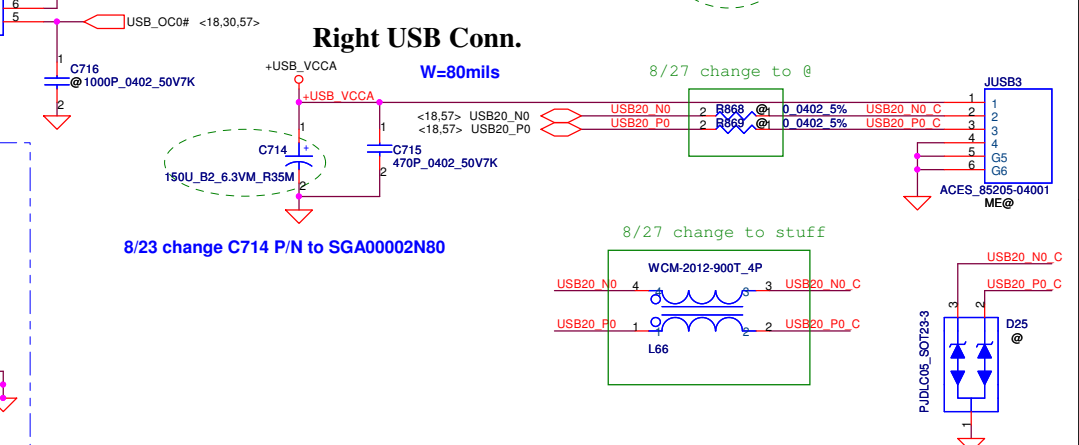
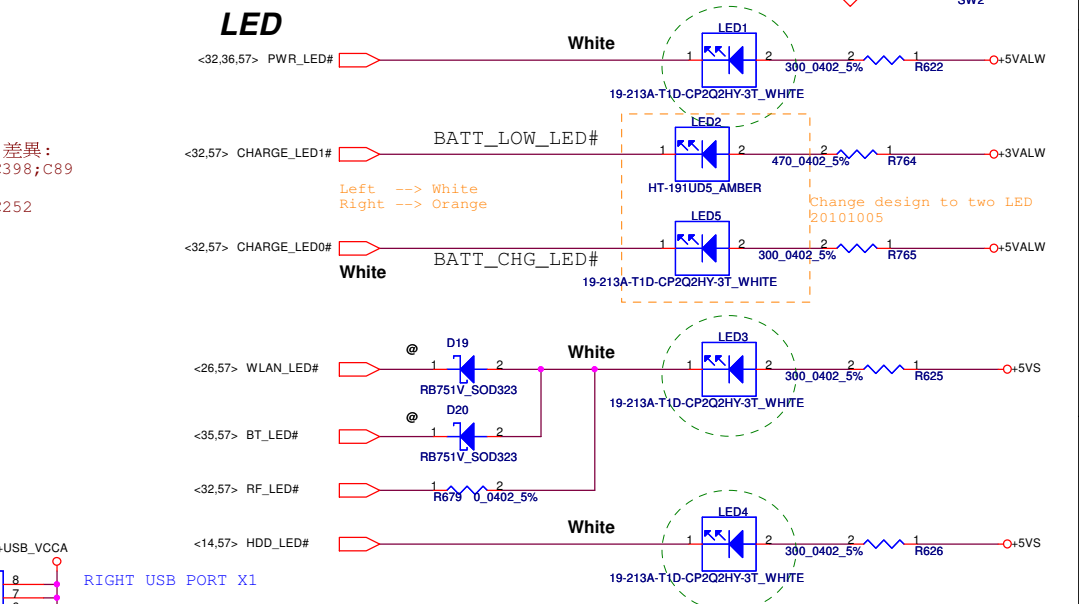
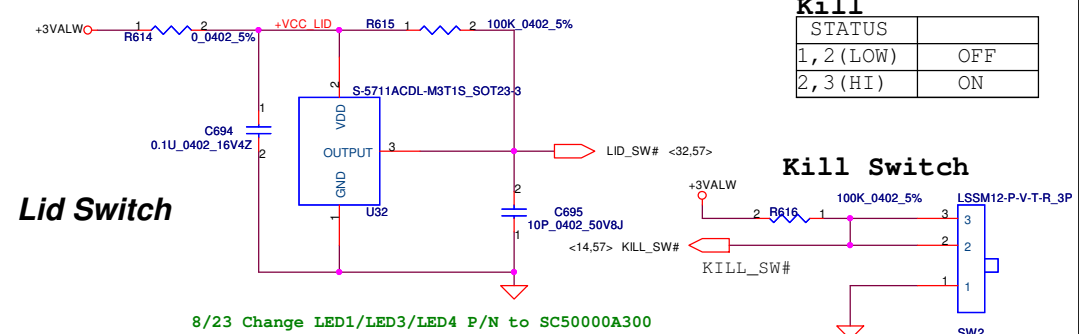
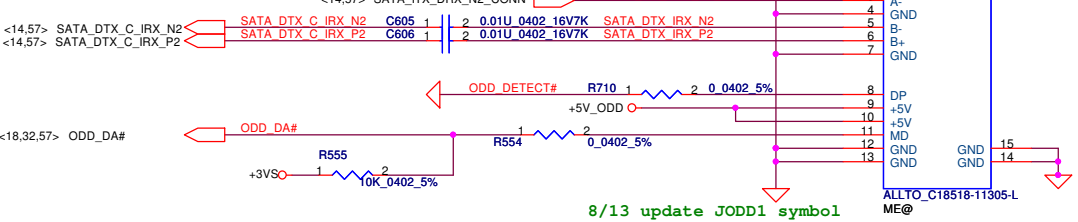
INT_KBD Conn.



CONN PIN define need double check



SATA ODD Conn.



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Issued Date	2010/07/12	Deciphered Date	2012/07/11	KB /SW /LPC Debug Conn.	
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				B	LA-6752P	0.2	
Date:				Friday, November 26, 2010	Sheet	58 of 60	

PHASE	PAGE	Modification list	PURPOSE
0.2	P16	D29 change to @	For AC detect issue
0.2	P24	R548,R549 change to DIS@	For AC detect issue
0.2	P10	C128 change to stuff	For test on DVI
0.2	P44	Del Q118, R657	For not need
0.2		Change R513, R516 ,R667 P/N and from 0805 to 0603	For common part
0.2		Change C633, C634 , C642	For common part
0.2		Change D3, D29 P/N and symbol	For common part
0.2		Change U3,U11,U13,U14,U38,U39 P/N and symbol	For common part
0.2		Change U3,U11,U13,U14,U38,U39 P/N and symbol	For common part
0.2		Change Q8,Q65,Q80,Q83,Q99,Q104 P/N and symbol	For common part
0.2		Change Q1,Q37,Q93 P/N and symbol	For common part
0.2		Change Q94, Q95 P/N and symbol	For common part
0.2		Change Q3,Q4,Q7,Q9,Q66,Q67,Q68,Q73,Q74,Q75,Q76,Q77,Q78, Q79,Q82,Q85,Q86,Q87,Q102,Q106,Q107,Q108,Q109,Q110,Q111,Q112,Q113,Q114,Q115,Q116 P/N and symbol	For common part
0.2		Change C635 part and change to @	For EMI
0.2	P18	Reserved R297	Reserved
0.2	P9	Change C53,C85,C86,C87 ,C397,C398,C399 to stuff and change ,C48,C80,C81,C82, C90,C91 to @ Del C89	For CPU_CORE
0.2	P10	Change C110,C111,C112,C113 to stuff	For VGFX_CORE
0.2	P56	Change LED1/LED3/LED4 P/N to SC50000A300	Change P/N
0.2	P36	Change T1,T2 P/N to SP050003N00	For test pass part
0.2	P40	Change R611,R740,C93 to stuff and change Y5,C347,C367 to @ Change R695 to 18K, Q37 change to @, R747 change to stuff,	For SUS_CLK R695 for Board ID, Q37, R747 for VR_HOT
0.2	P40	Change U33 P/N to SA00003FL10	For BIOS ROM
0.2		Change C509,C511,C635 to stuff	For EMI
0.2	P56	Change I4" C714 P/N to SGA00002N80	For Sourcer request
0.2	P39	Change R720,R721,R722,R723 P/N to SM01000BZ00(Bead), and Change C647,C649,C650,C651 to Stuff	For EMI request
0.2	P19	Change R303 to Stuff, and change R542 to @	For BIOS ESATA detect function
0.2	P56	Change U32 P/N to SA000031C00	For common part
0.2	P36	Change T1,T2 P/N to SP050006E00	For correct part
0.2	P10	R688 change to stuff , R687 ,Q7 change to @	For S3 power reduction
0.2		Change R660,R661,R862,R863,R864,R865,R868,R869 to @ , change L63,L64,L65,L66 to stuff , change R619 to Bead (SM01000DI00)	For EMI
0.2	P20	Change L75 symbol	For common part
0.2	P30	Change R402 to @	For DPST
0.3	P10	Update Q5 symbol	For update symbol
0.3	P33	Add F2	For safty request
0.3	P39	Update U30 P/N to SA00003K410 and Add R879	For Audio update to 21Z
0.3	P10	Change C128 to D2 size and @	Change size for M/E issue
0.3	P14	Add reserve R878	For Intel DG 1.5
0.3	P37	C592 change P/N to SF000001500 (H=6)	For ME Z high ok
0.3	P29	R369 P/N change to SD034100A80	For GP part
0.3	P6	Reserved R880 to SYS_PWR0K	Follow ORB
0.3	P10	R62,R63 change to 1K	Follow CRB
0.3	P33	R483,R484 change connect to +5V_HDMI_F	For Add F2
0.3	P37	Change U27 P/N to SA000046C00	For Fintek
0.3	P40	Change R594 pull high to +5VALW	For leakage issue

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PHASE	PAGE	Modification list	PURPOSE
0.3	P19	R881 change to D ₁ uff, R244 change to @	For intel MRC Rev0.9
0.3	P14	R878 change to stuff	For intel DG 1.5
0.3	P31	Del R432	For non-used part
0.3	P36	Reserved D31 , C643 , C644	For reserved EMI parts
0.3	P37	Del R581	For non-used part
0.3	P38	Del R550	For non-used part
0.3	P38	Change C592 P/N to SF0000002Y00	For M/E Z high limit
0.3	P39	Del R584, R586 , R587	For non-used part
0.3	P40	Change R600, R604 to 2.2K Change R695 to 8.2k	Change R600, R604 for Battery SMBus, R695 for Board ID
0.3	P42	Del R583	For non-used part
0.3	P31	Del R449, R452, R458, R460 (UMA change only)	For non-used part
0.3	P32	Del R478, R480, R486 (UMA change only)	For non-used part
0.3	P6	Reserved R882 connect to PCH_PWROK	Reserved for intel
0.3	P56	R765 change to 300 ohm	For LED

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				Date:	Friday, November 26, 2010
				Sheet	60 of 60